Physical Design of Digital Integrated Circuits (EN0291 S40)

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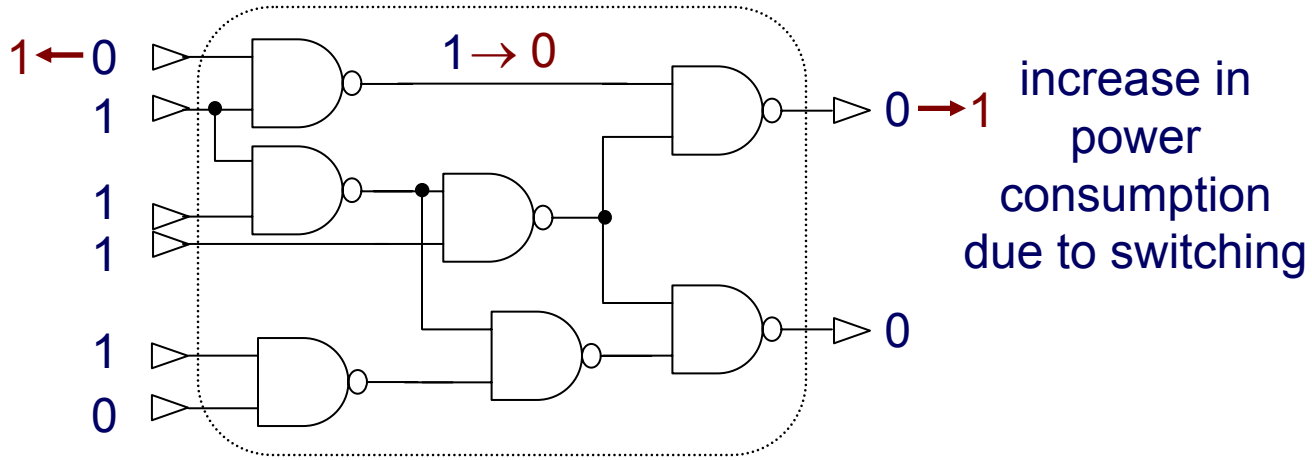
Lecture 06: Power Analysis and Reduction

- Power Analysis
- Power Optimizations: Dynamic
- Power Optimizations: Leakage
- Impact of Variability on Power

Total power = dynamic + standby (leakage)



Static/leakage/standby power: power dissipated when no switching occurs

Dynamic power: power dissipated when circuit switches due to signal transition

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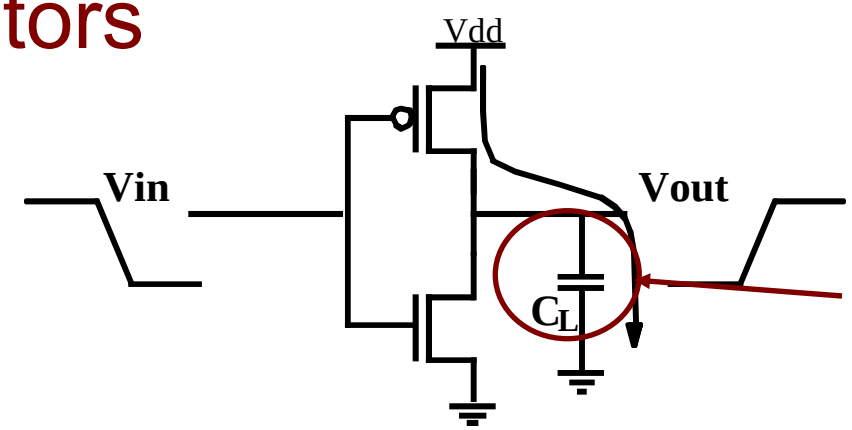
Dynamic power due to charging/discharging of capacitors



load capacitance (gate + diffusion + interconnects)

Energy delivered by the supply during input 1 → 0 transition:

$$E_{VDD} = \int_0^\infty i_{VDD}(t) V_{DD} dt = V_{DD} \int_0^\infty C_L \frac{dv_{out}}{dt} dt$$

$$E_{VDD} = C_L V_{DD} \int_0^{V_{DD}} dv_{out} = C_L V_{DD}^2$$

Energy stored at the capacitor at the end of 1 → 0 transition:

$$E_C = \int_0^\infty i_{VDD}(t) v_{out} dt = \int_0^\infty C_L \frac{dv_{out}}{dt} v_{out} dt$$

$$E_C = C_L \int_0^{V_{DD}} v_{out} dv_{out} = \frac{C_L V_{DD}^2}{2}$$

dissipated in NMOS during discharge (input: 0 → 1)

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Capacitive dynamic power

- If the gate is switched on and off $f_{0\rightarrow1}$ (switching factor) times per second, the power consumption is given by

$$P_{dyn} = C_L V_{DD}^2 f_{0\rightarrow1}$$

- For entire circuit

$$P_{dyn} = \sum_i \alpha_i C_{L_i} V_{DD}^2 f$$

where α_i is activity factor [0..0.5] in comparison to the clock frequency

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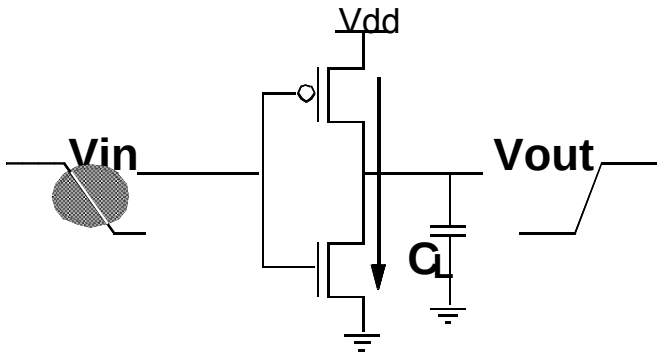
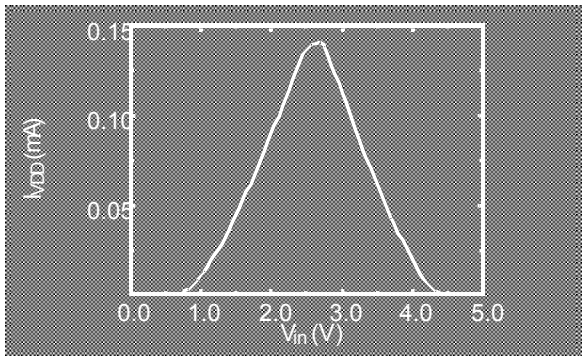
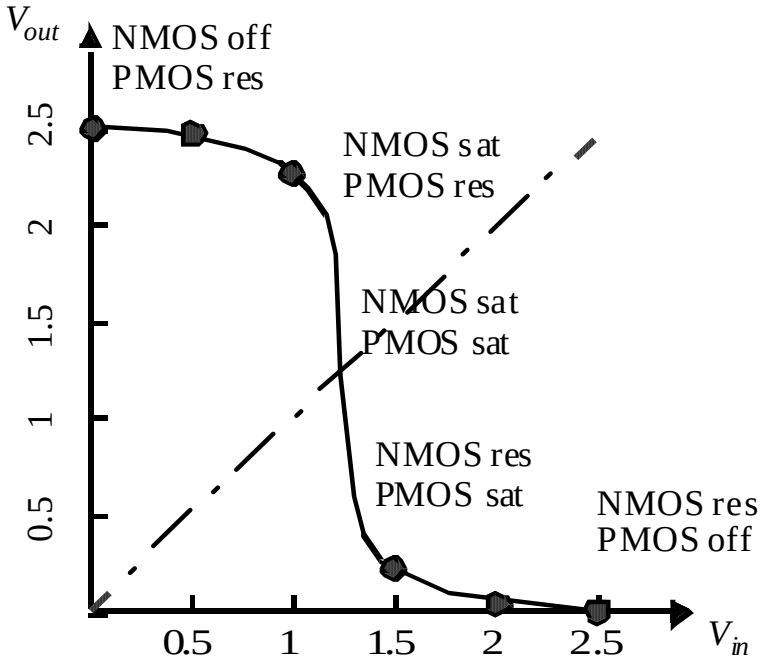
Dynamic power: short circuit power







- Short circuit power occurs during transition period when both the NMOS and PMOS transistors are on
- Short circuit current is typically < 10%

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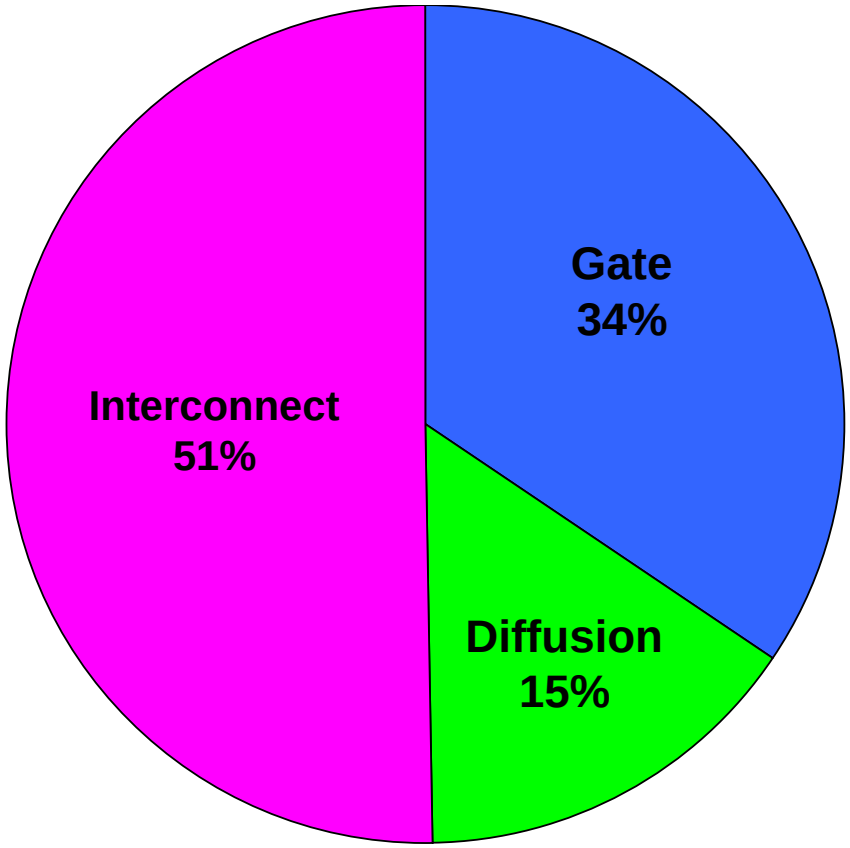
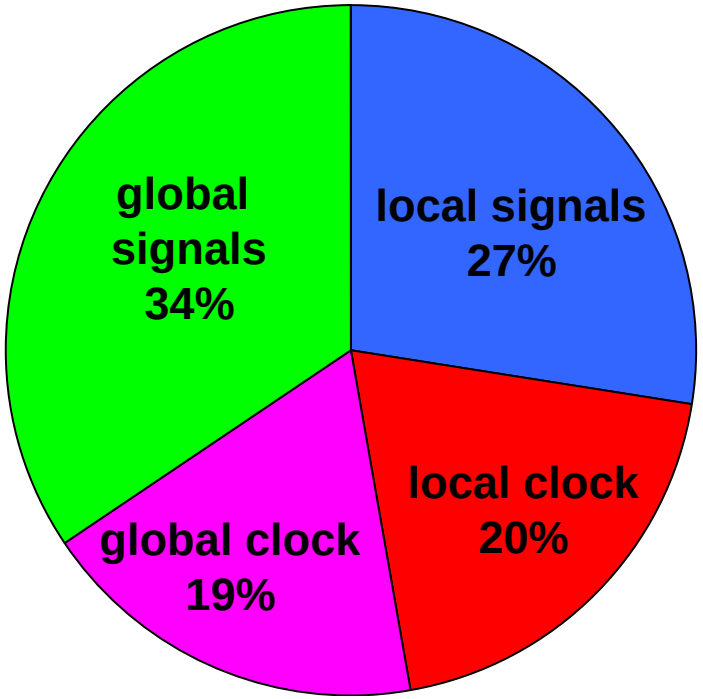
Dynamic power breakup



Total dynamic Power



Interconnect Power

[source: Intel'03]

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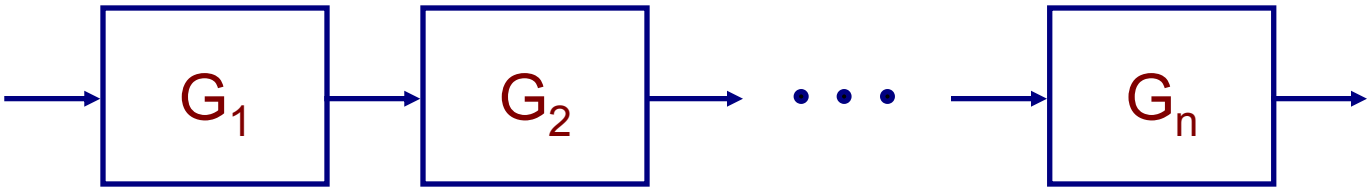
1. Gate power reduction via transistor sizing



Increasing transistor sizes (width):

- reduces effective output resistance
  - $\rightarrow$ reduces time to drive a load
- increases transistor capacitance
  - $\rightarrow$ slows down previous stage
  - $\rightarrow$ increases dynamic power

Transistor-Sizing Optimization Problem (given a circuit):

Objective: size all transistors to minimize total power

Constraint: meet timing constraints

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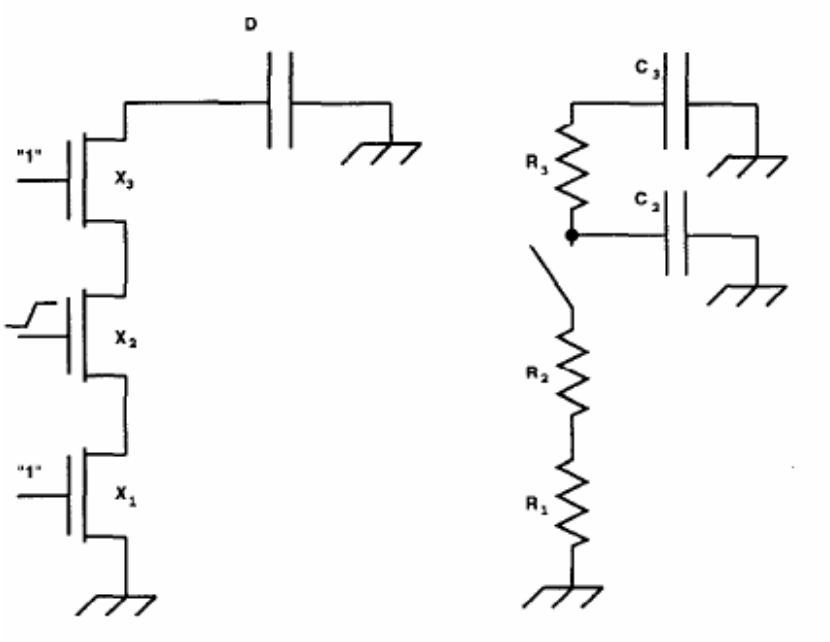
1. Transistor-sizing problem



Let X_i be the transistor sizes

$$delay = (R_1 + R_2)C_2 + (R_1 + R_2 + R_3)C_3$$

$$delay = (\frac{A}{X_1} + \frac{A}{X_2}) \times (BX_2 + BX_3 + C) + (\frac{A}{X_1} + \frac{A}{X_2} + \frac{A}{X_3}) \times (BX_3 + D)$$

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2. Interconnect power reduction via sizing

- Increasing wire width / thickness
  - increases capacitance → increases dynamic power
  - reduces resistance → reduces delay
- Increasing spacing between wires
  - reduces capacitance → reduces dynamic power
  - takes more area

    → causes congestion and increase capacitance somewhere else

Wire-Sizing Optimization Problem (given placed circuit):
Objective: size all wires to minimize total power
Constraint: meet timing constraints

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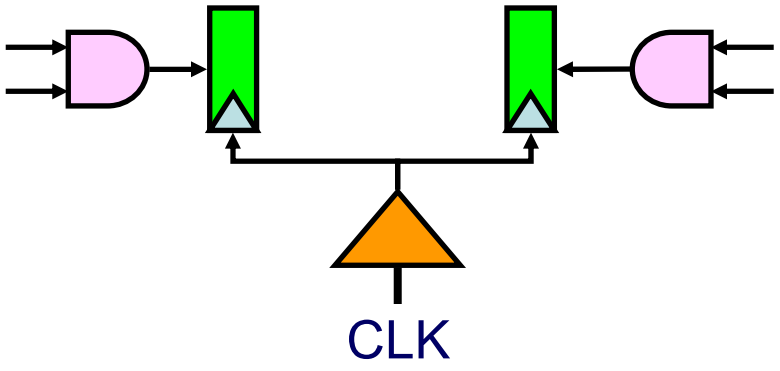
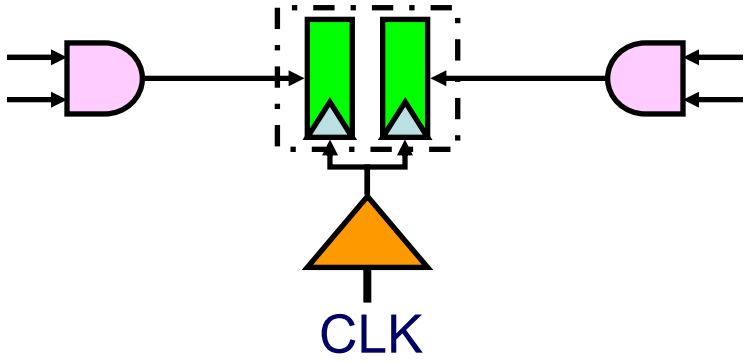
3. Power-driven Interconnect P & R

Q: If clock nets consume ~ 40% of total dynamic power, how can we reduce their power as well as total system power?

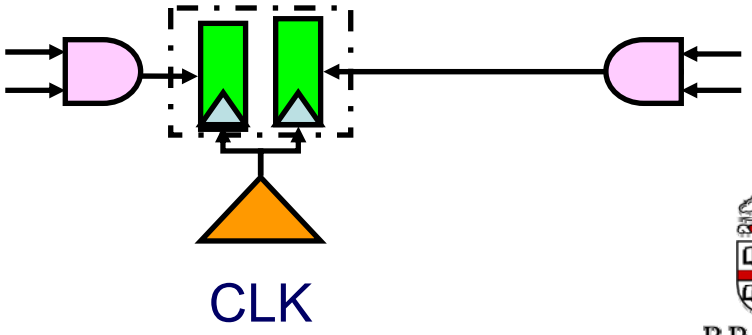


1. tweak placement to reduce clock tree length



2. tweak placement to optimize wire lengths depending on their switching activity

$\Rightarrow$ improves total dynamic power with little impact on timing



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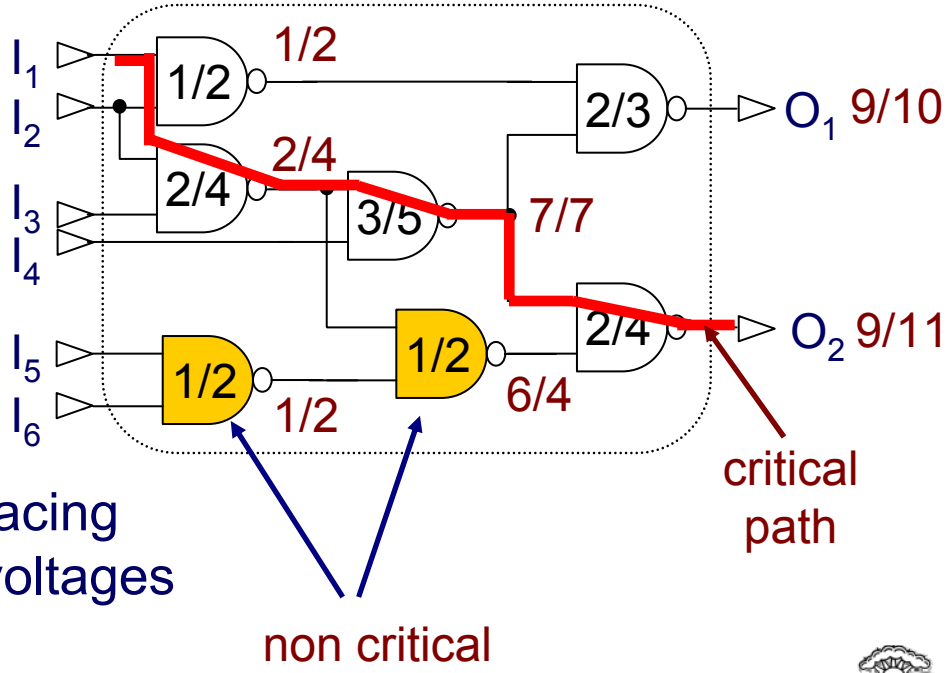
4. Dynamic power reduction via multiple V_{dd}

Dynamic power is proportional to square the supply voltage $P_{dyn} = \sum_i \alpha_i C_{L_i} V_{DD}^2 f$

$\Rightarrow$ reducing supply voltage reduces power but increases delay

Only reduce supply voltage of non critical cells



Problems:

- Two supply networks
- Voltage converters when interfacing subcircuits with different supply voltages

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5.Dynamic power reduction via dynamic V_{DD} scaling

- Scaling down supply voltage
  - reduces dynamic power
  - reduces saturation current

    $\rightarrow$ increases delay $\rightarrow$ reduce the frequency

Dynamic voltage scaling (DVS): Supply and voltage of the circuit should dynamic adjust according to the workload of our circuits and criticality of the tasks

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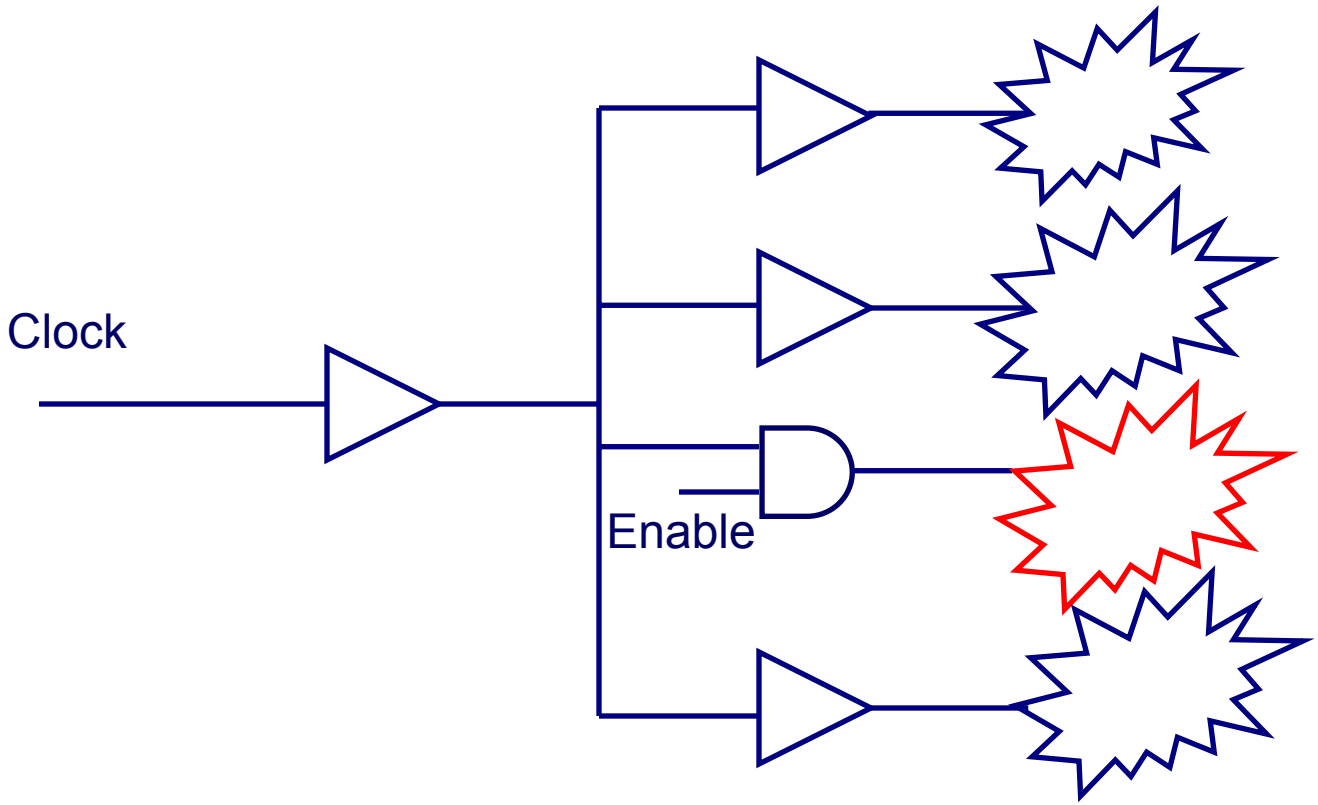
6. Clock tree gating to reduce dynamic power



- Since clock accounts for large fraction of total power, *clock gating,* gates the clock signal from idle subcircuits (units) saving lots of power

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Lecture 06: Power Analysis and Reduction

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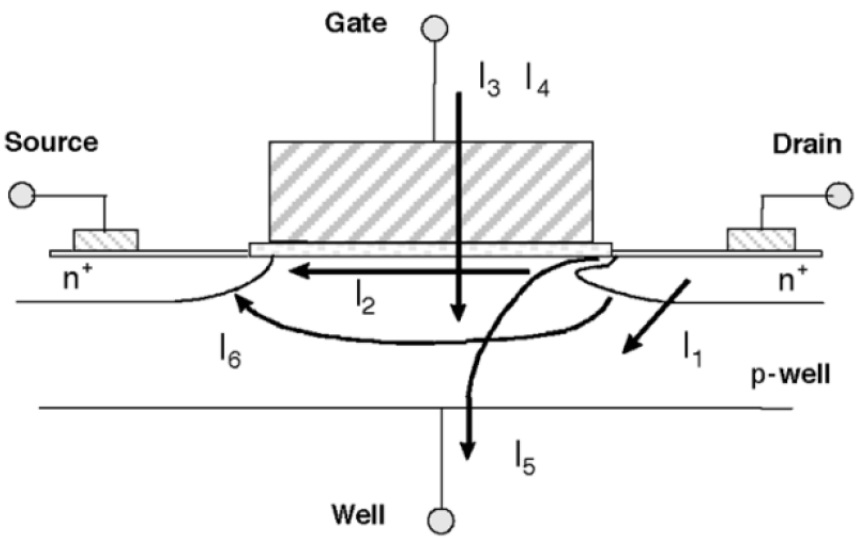
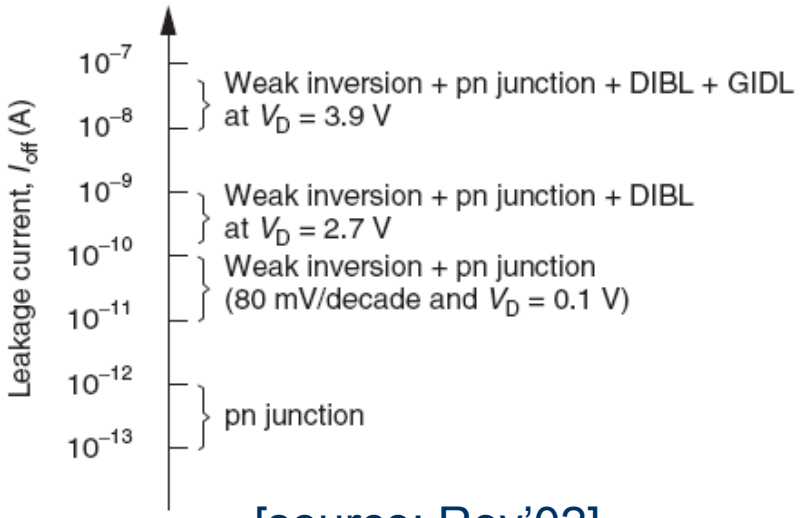
Leakage current components





[source: Roy'02]

- I_1: pn junction reverse-bias current
- I_2: subthreshold leakage (weak inversion) $I_{sub} = KWe^{\frac{-V_{th}}{nT}}(1 - e^{\frac{-V_{DS}}{T}})$
- I_3: Gate tunnel current
- I_4: Hot carrier current
- I_5: Gate-Induced Drain Leakage
- I_6: Punch-through current

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1. Leakage reduction via transistor stacking

When M_1 and M_2 are both turned off:

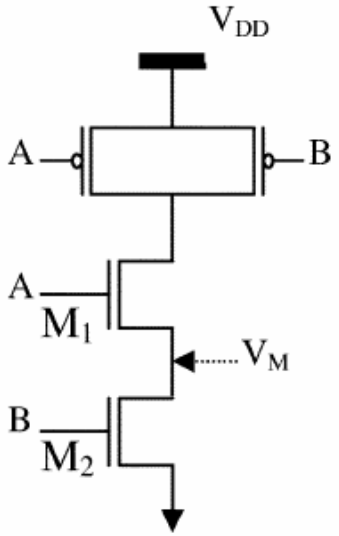
→Current through M1 and M2 increases $V_M > 0$

→ $V_{GS} = V_{GM}$ becomes negative

→ Subthreshold current reduces

→ V_{bs} of M_1 becomes negative reduces V_t of M_1

→ reduces leakage current



Leakage of a two-transistor stack is an order of magnitude less than leakage in a single transistor

→ Dependence of leakage current on the state of the inputs (L[00], L[01], L[10], L[11])

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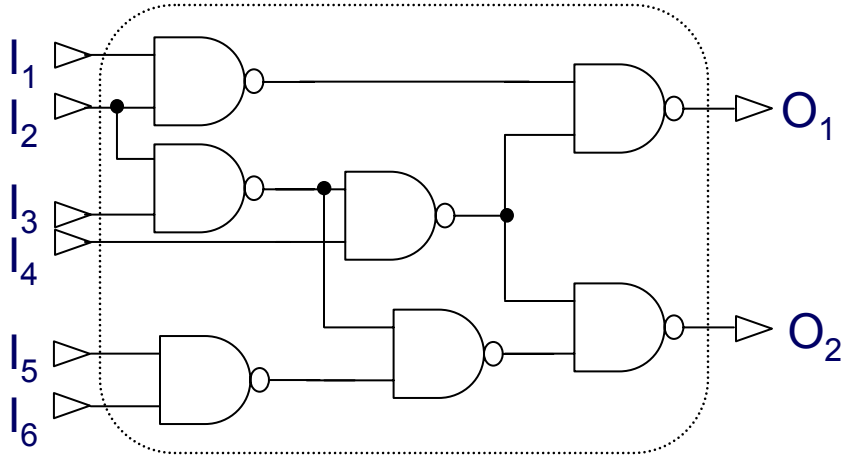
1. Leakage reduction via PI setting

C17 from ISCAS'85 benchmarks



Problem: Find a primary input vector (n bits) that would minimize the total standby leakage current?

Heuristic solutions are in assigned readings!

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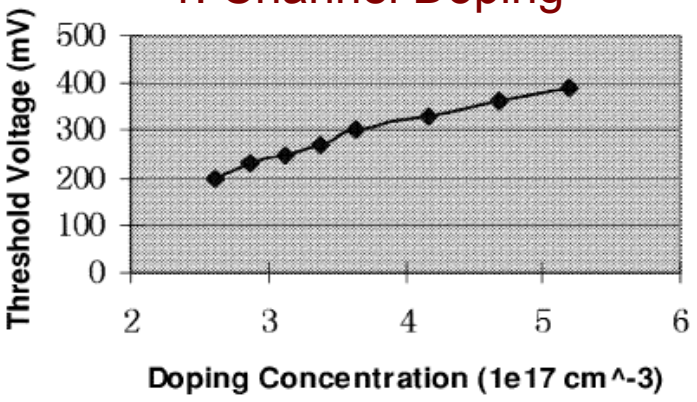
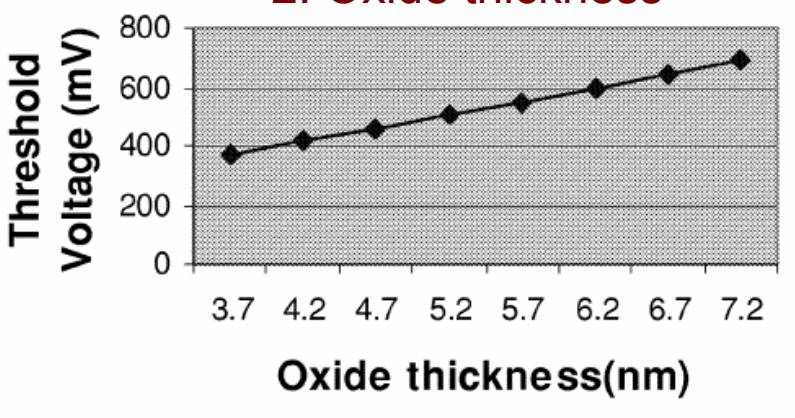
2. Leakage reduction via adjusting of V_{th}

- Leakage depends exponentially on V_{th}. How to control V_{th}?
  - Remember: V_{th} also controls your saturation current → delay

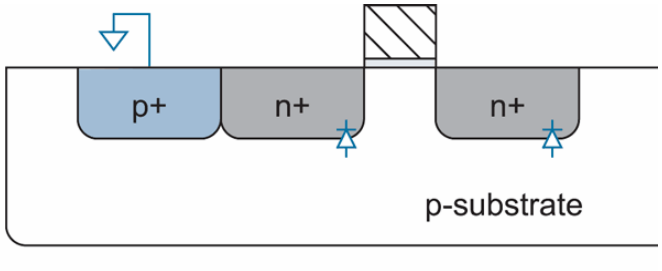
1. Channel Doping



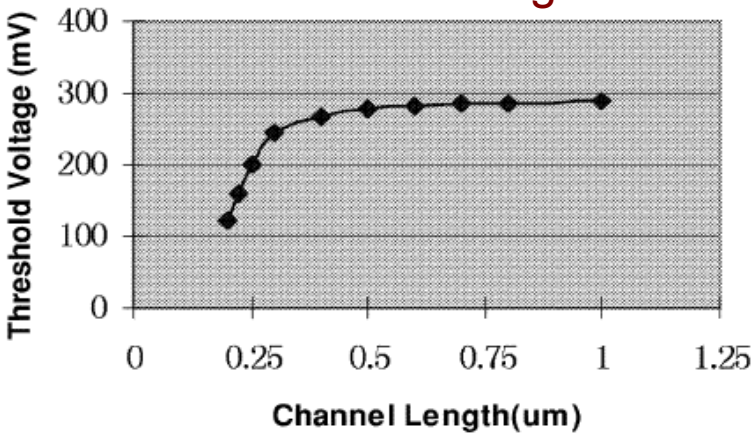
2. Oxide thickness



4. Body Bias



3. Channel length



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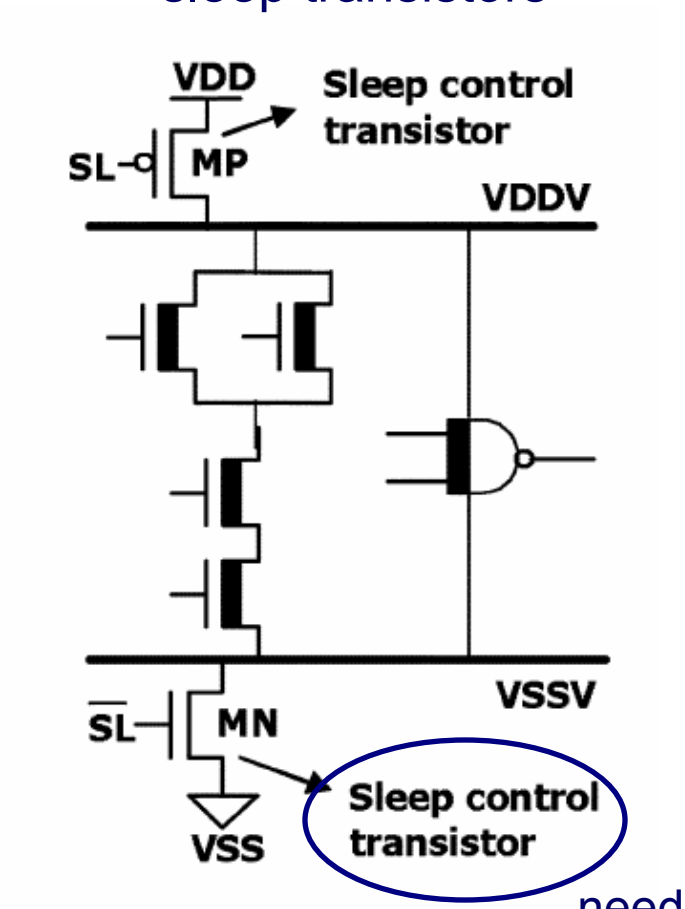
2. Leakage reduction via the use of multiple V_{th}

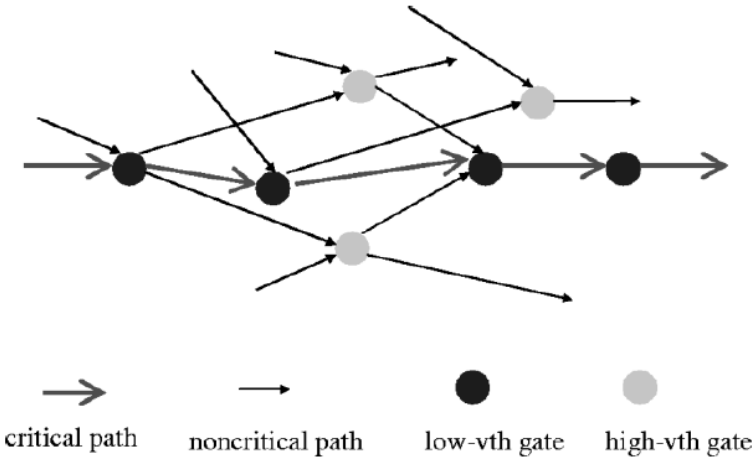
A. High-threshold sleep transistors



[Figure: Roy'03]

needs to be properly size

B. Dual threshold CMOS



Assign high V_{th} cells to non-critical cells; low V_{th} to critical path cells

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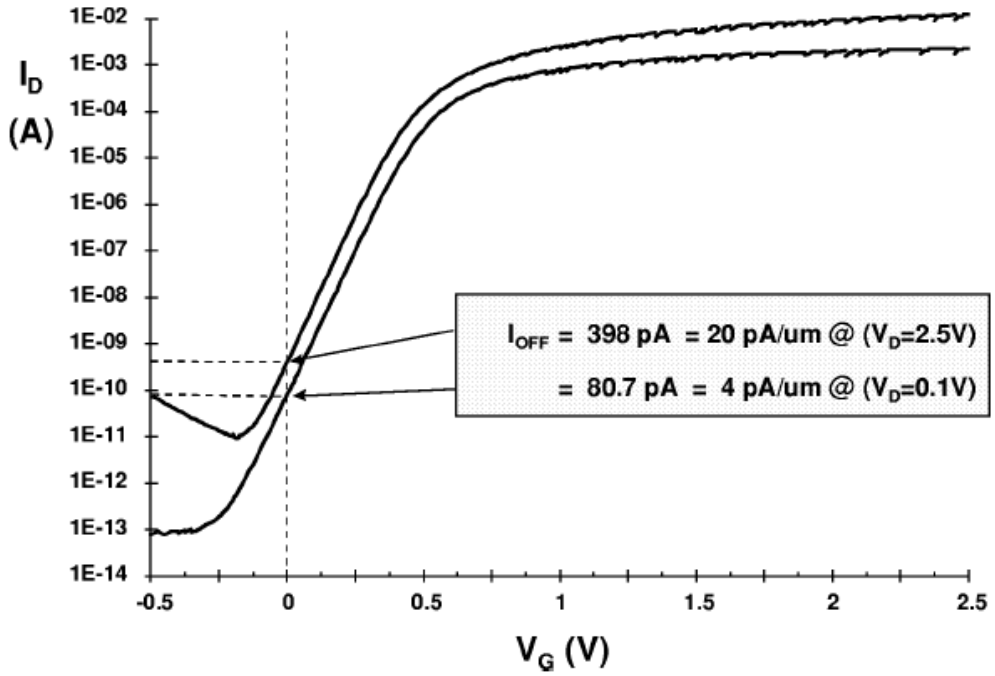
3. Leakage reduction via V_{DD} Scaling



In short-channel transistors:

- Scaling supply voltage reduces V_{th} (Drain Induced Barrier Lowering DIBL)
- Reducing V_{th} increases leakage

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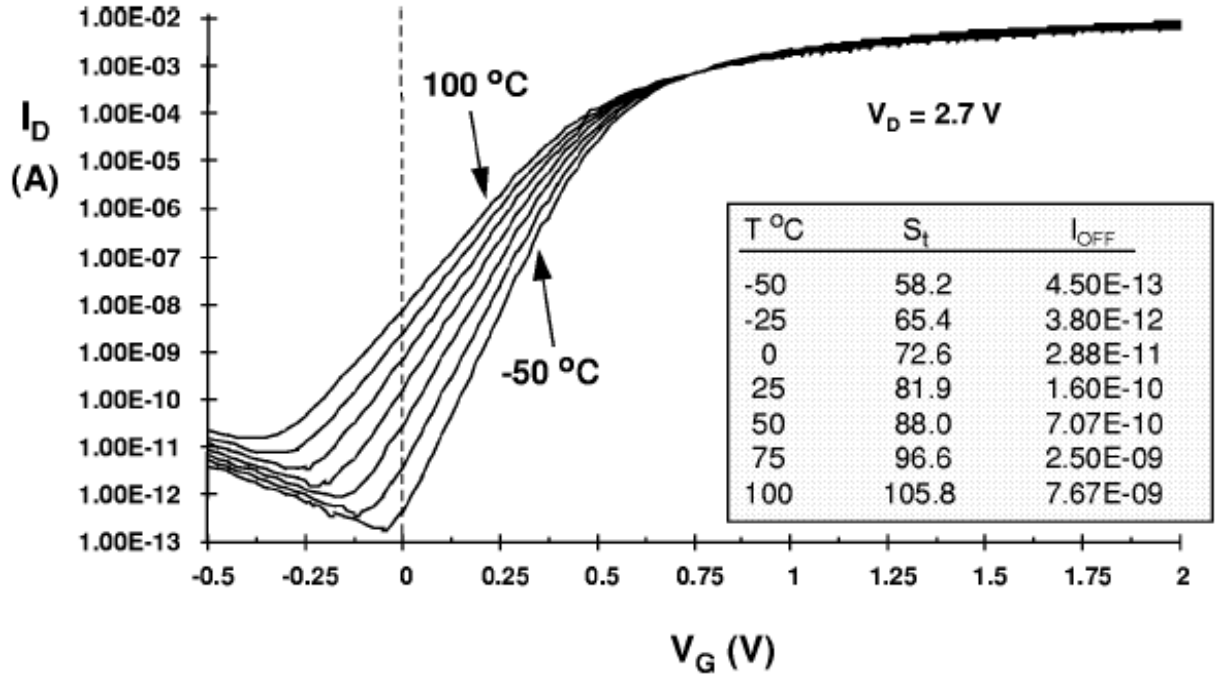
4. Leakage reduction via Cooling



T °C	S_t	I_{OFF}
-50	58.2	4.50E-13
-25	65.4	3.80E-12
0	72.6	2.88E-11
25	81.9	1.60E-10
50	88.0	7.07E-10
75	96.6	2.50E-09
100	105.8	7.67E-09

- Impact of temperature on leakage current

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Lecture 06: Power Analysis and Reduction

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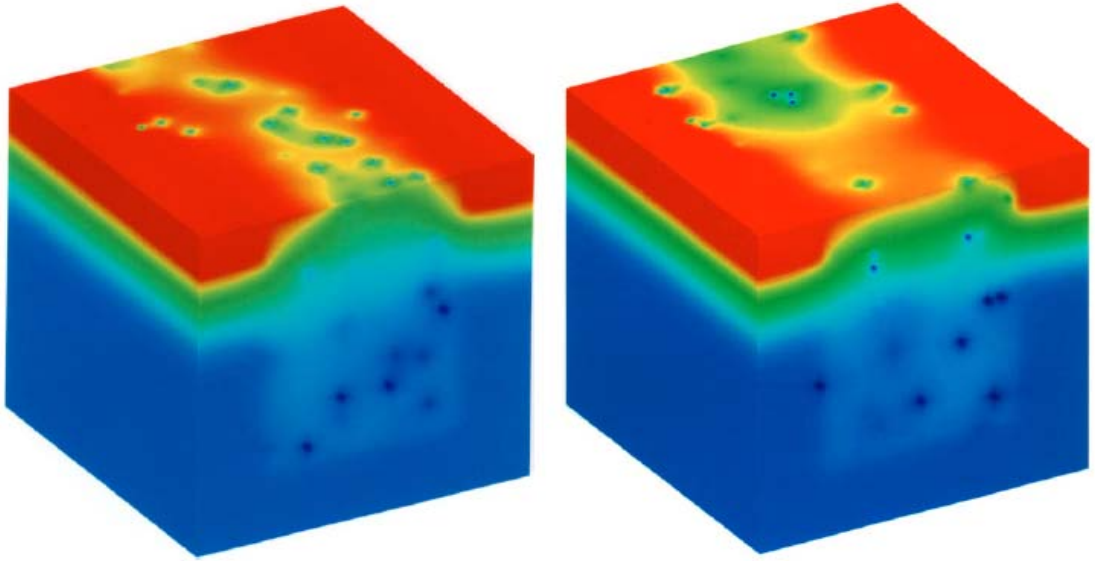
Impact of V_{th} variations on power

Both MOSFETs have 30nm channel with 130 dopant atoms in the channel depletion region



Different dopant profiles alter V_{th}

threshold voltage 0.97V

threshold voltage 0.57V

[source: Asenov'99]

- Below-nominal values for threshold voltage increases leakage currents

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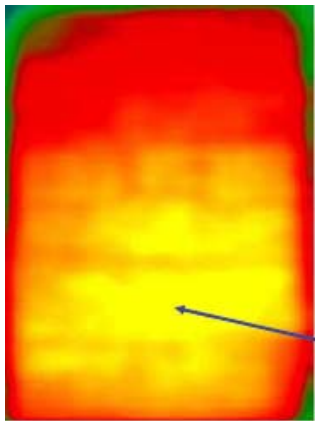
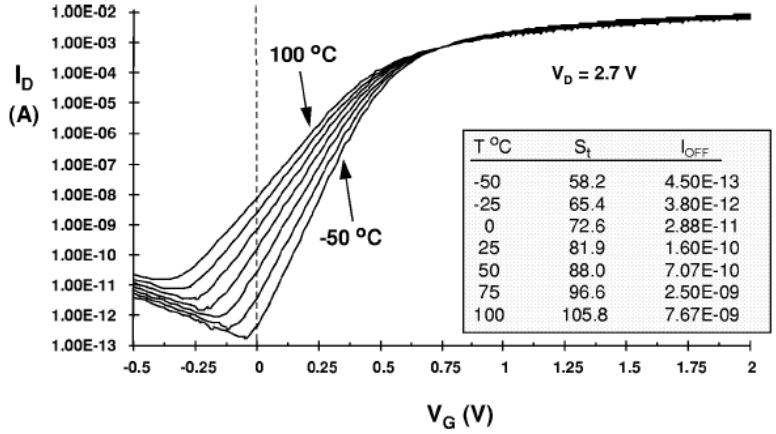
Impact of temperature variations on power

Temperature profile of PowerPC 970 [Rohrer'04]



Impact of temperature on leakage current



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50	88.0	7.07E-10
75	96.6	2.50E-09
100	105.8	7.67E-09

- Runtime Variations in temperature increases leakage current (compared to leakage @ room temperature).
- Increases in leakage current lead to further increases in temperature!

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Assigned Readings

- Short-Circuit Dissipation of Static CMOS Circuitry and its
- Impact on the design of Buffer Circuits [Veendrick'84]
- Elif

- Adaptive Body Bias for Reducing Impacts of Die-to-Die and within-dir parameter variations on up frequency and leakage Nuno

- Wattch: A Framework for Architectural-Level Power and Analysis and Optimizations Yiwen

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