Physical Design of Digital Integrated Circuits (EN0291 S40)

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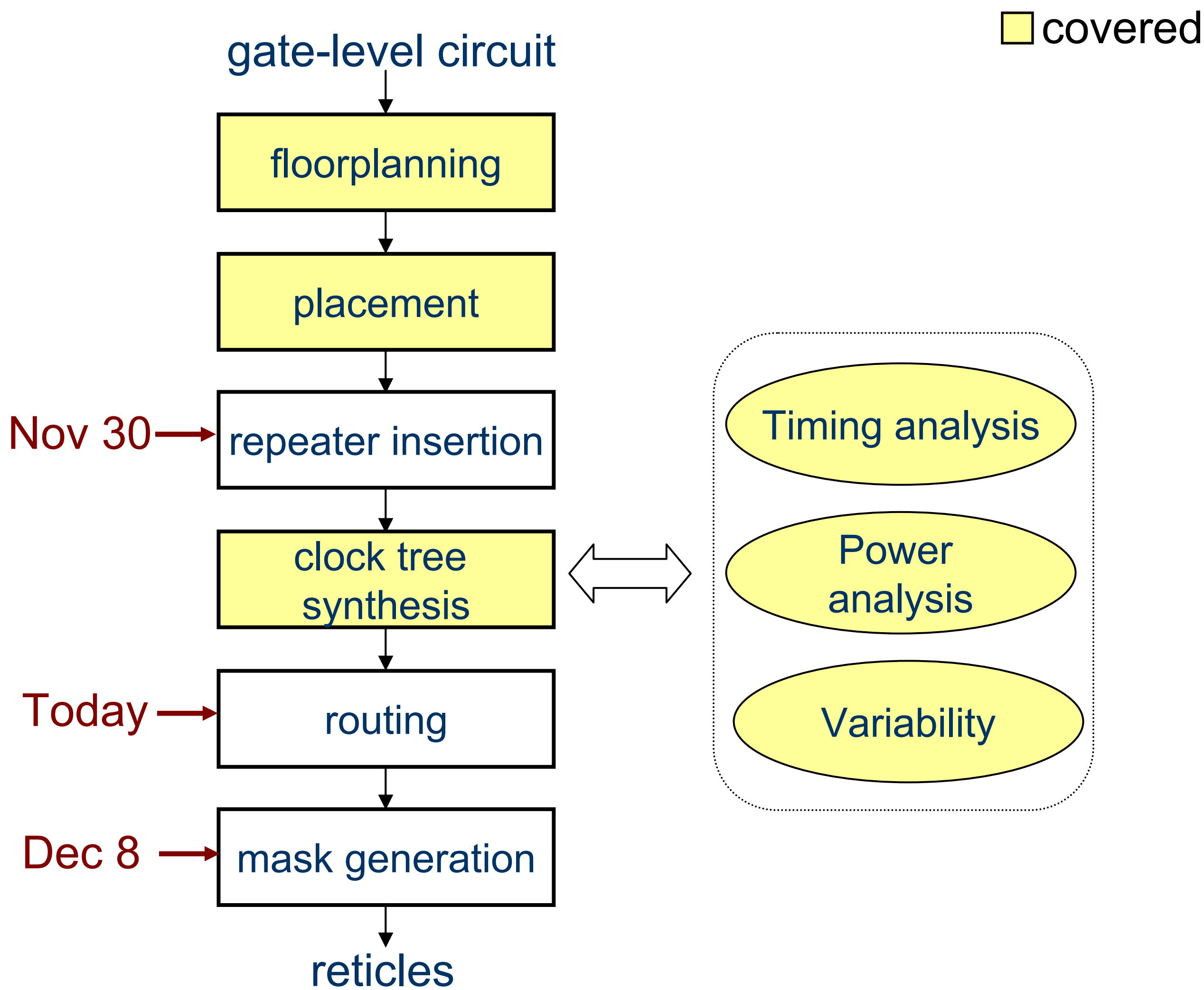
Lecture 09: Routing

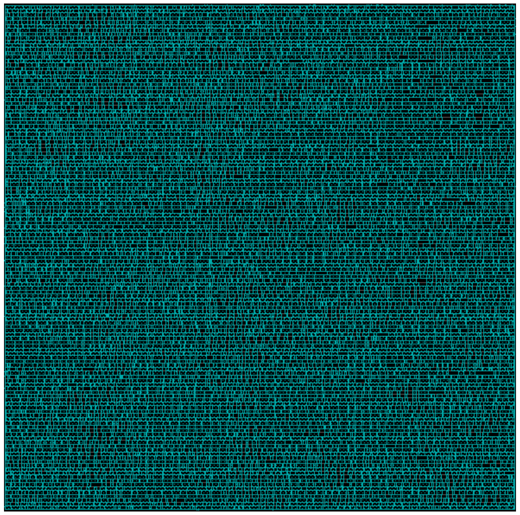
- Introduction to Routing
- Global Routing
- Detailed Routing

Current status in our physical design class

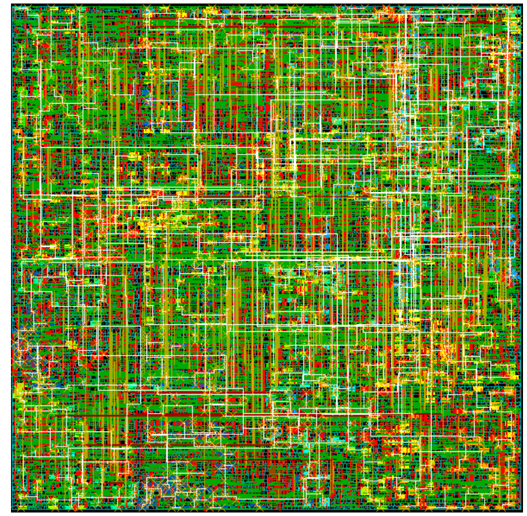


Routing objectives

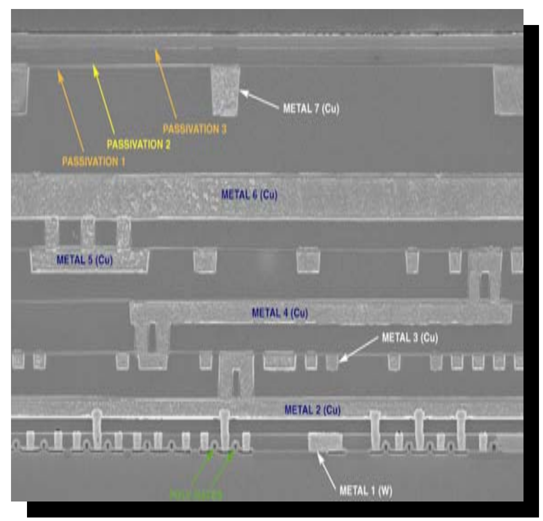
placement



Routed placement - a top view



Routed placement - a cross sectional view



Given a placement and a stack of metal layers, find a routing (metal segments/vias/contacts) for each net while

- minimizing total routing metal
- meeting timing objective

And such that…..

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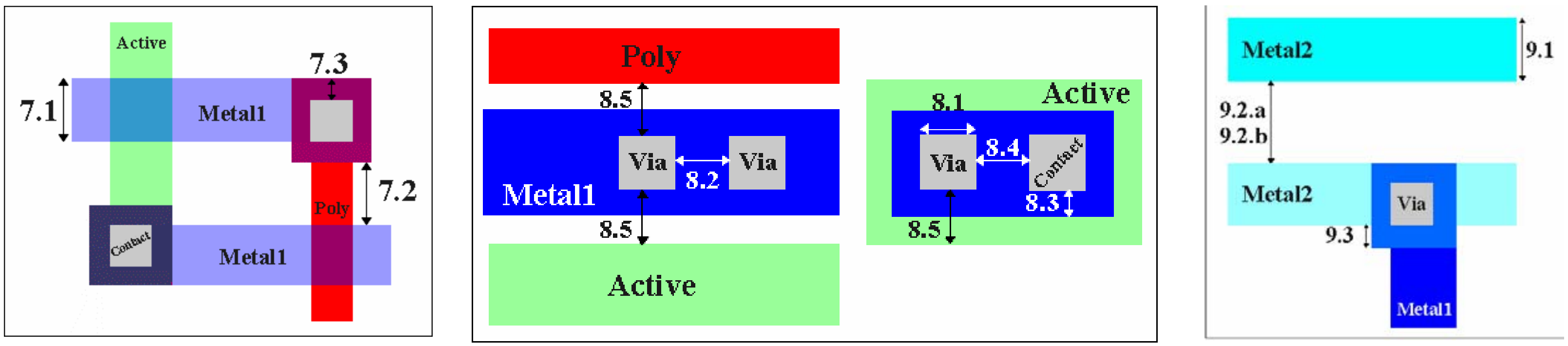
Routing constraints

- Design rules must be met, which include
  - Minimum spacing between metal tracks
  - Minimum wire widths
  - Spacing between vias/contacts and segments



Sample MOSIS design rule

- Routing is not easy!
  - Greater than 1 million nets designs are common
  - 20×20 mm chip with 100nm rules and a pitch of 200nm
    - 10^5 tracks across
    - $10^5 \times 10^5 \times 10 = 10^{11}$ grid points!

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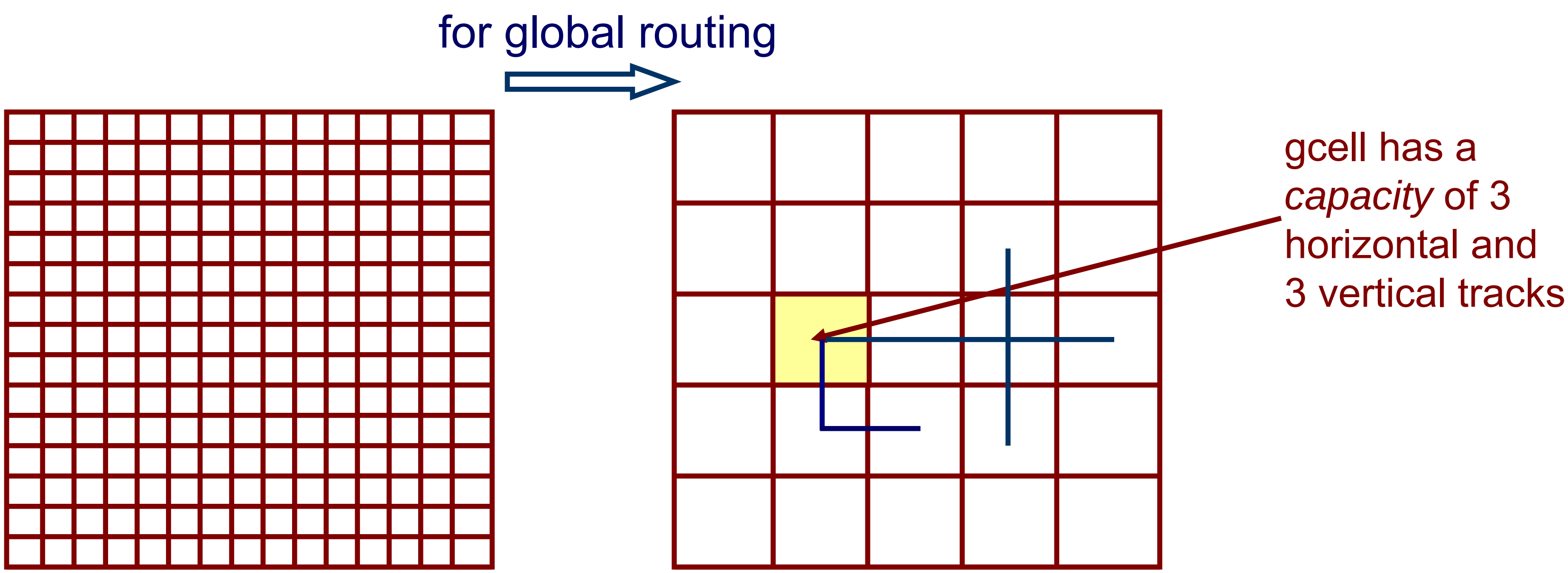
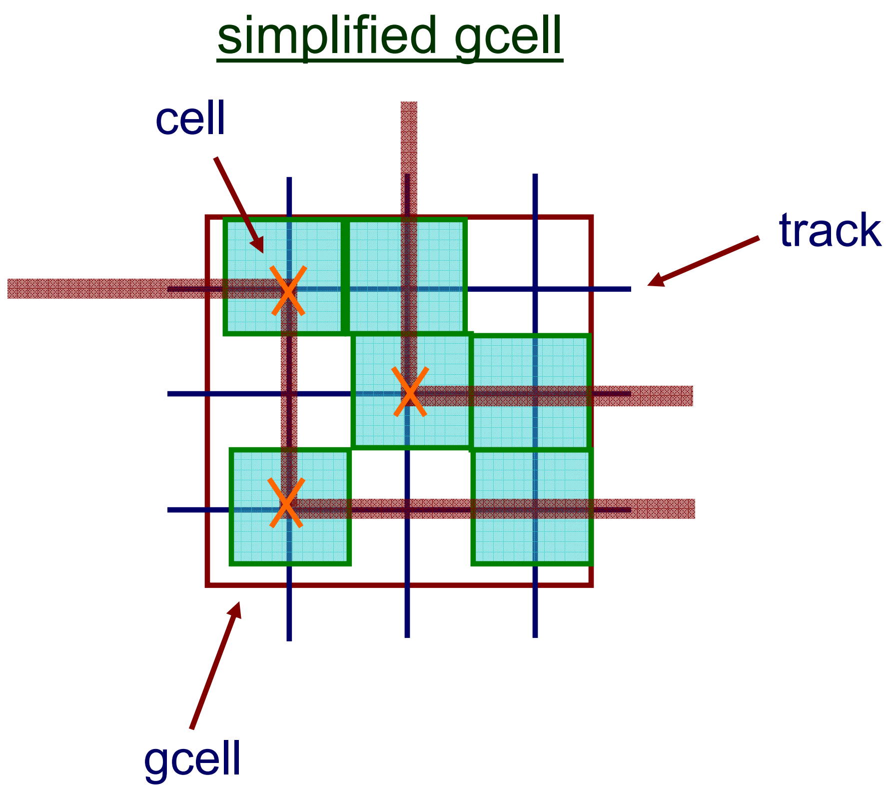
Routing can be overwhelming → divide into global and detailed

- Because the problem size can be overwhelmingly large, routing is typically divided into two steps: global and detailed



Construct a coarse grid
Consider all cells inside gcell in its center
Construct routes such that capacities are not violated

Detailed routing maps out the exact route (metal segments + vias) used by a route



- Detailed routing takes as an input the global route of each net including each gcell the net enters/exits

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Global routing techniques

- Sequential approaches
  - Considers one net at a time → sensitive to ordering
  - How to order nets for routing?
- Concurrent approaches
  - Considers all nets at the same time ← not covered!
  - Computationally harder and does not scale well

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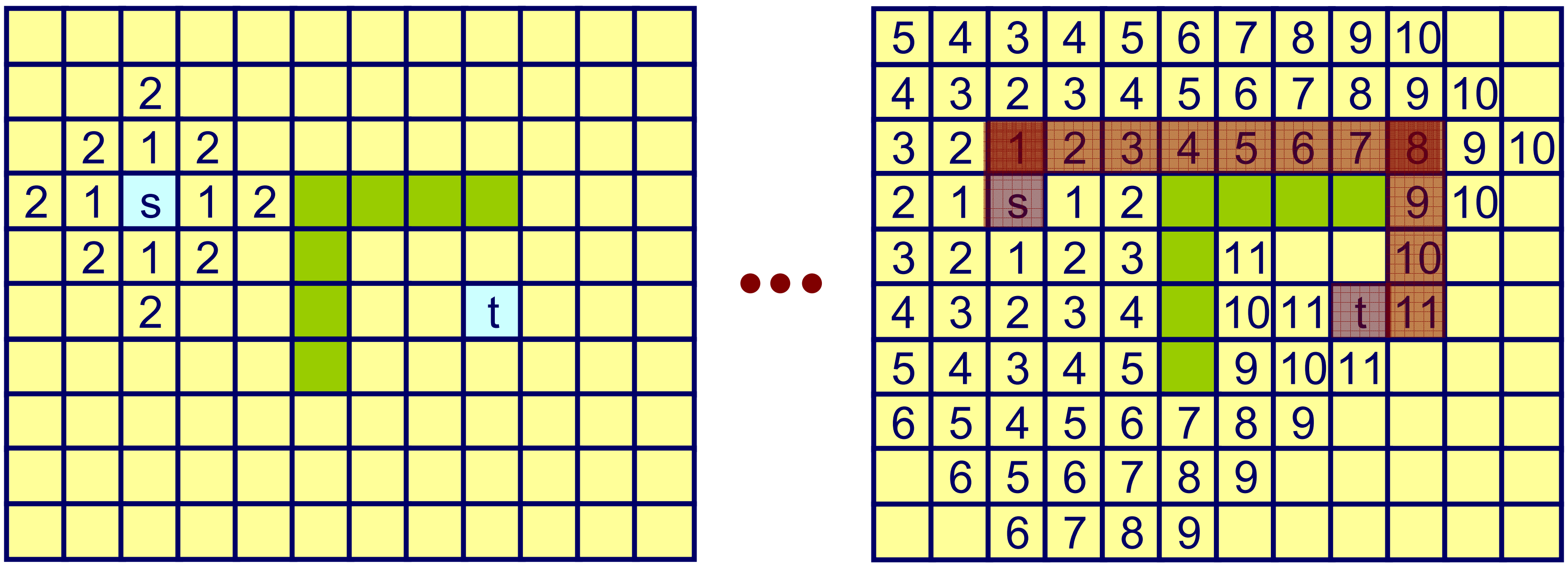
How to find the shortest path between two points on the global routing grid?

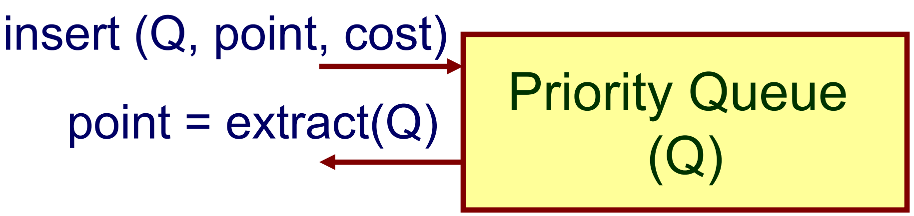


<u>Problem:</u> Find the shortest path for a 2-pin wire from s to t

- grid cell capacity is full
- grid cell still has available tracks

<u>Solution:</u> Maze algorithm

Maze Algorithm



If there are n elements in the queue:

- ➢insertion cost is O(log n)
- ➢extraction cost is O(log n)

```
Initialize priority queue Q, and insert s with cost 0
repeat
  x = extract (Q)
  Let N be the neighbors of x
  for each neighbor y: insert(Q, y, cost(x)+cost(x→y))
Until x == T or Q is empty
```

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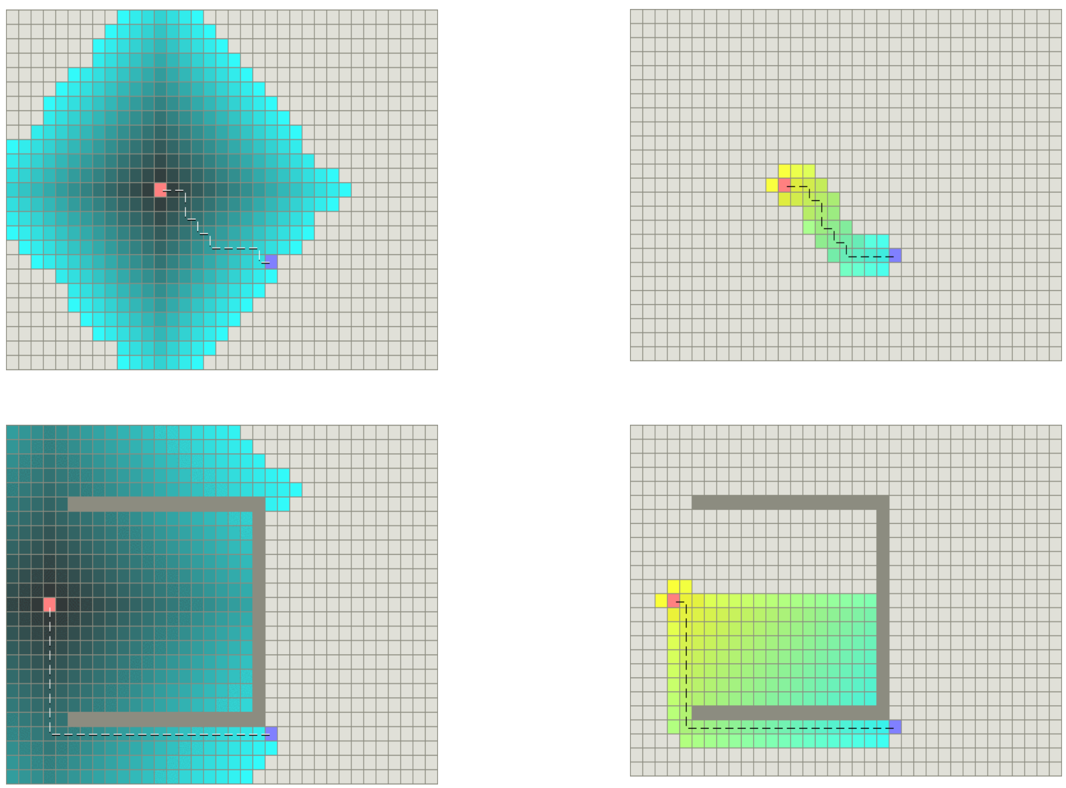
Speeding up the search (A* algorithm)

- Cost of point y = cost(s → x) + cost(x→y) + lower bound (y → t)
  (s and t are the start and end points respectively)
- *What could be a simple lower bound?*

maze search | A* search



[Example from Prof. D. Pan Lecture]

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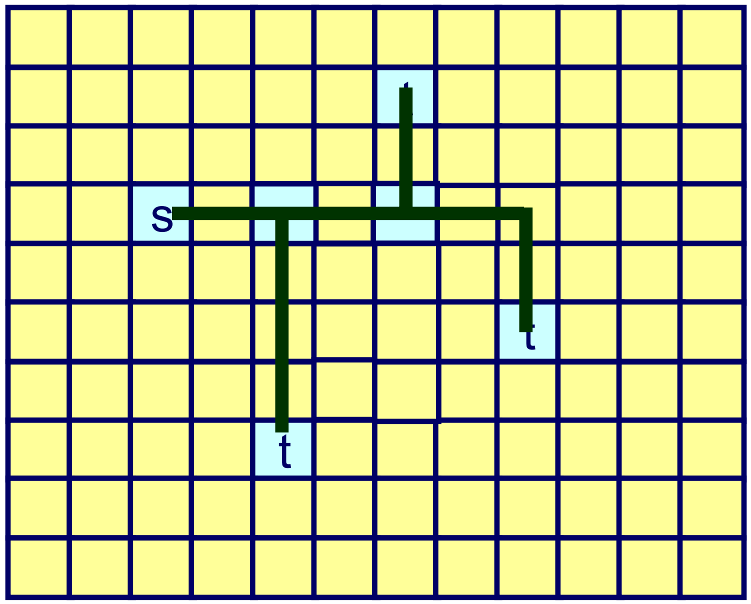
How to deal with multi-pin nets?

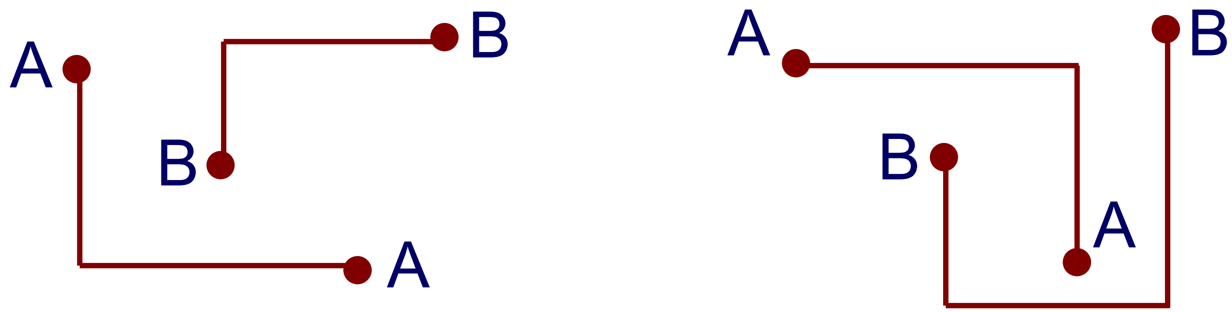


- Construct the Steiner “minimum” tree
- Label out the Steiner points
- Use the Steiner points to decompose the tree into two-pin wires
- Route each two-pin wire using maze-routing

Impact of Net Ordering

- A bad net ordering
  - may unnecessarily increase the total wirelength
  - or even yield the chip unroutable!

- Example: Two nets A and B

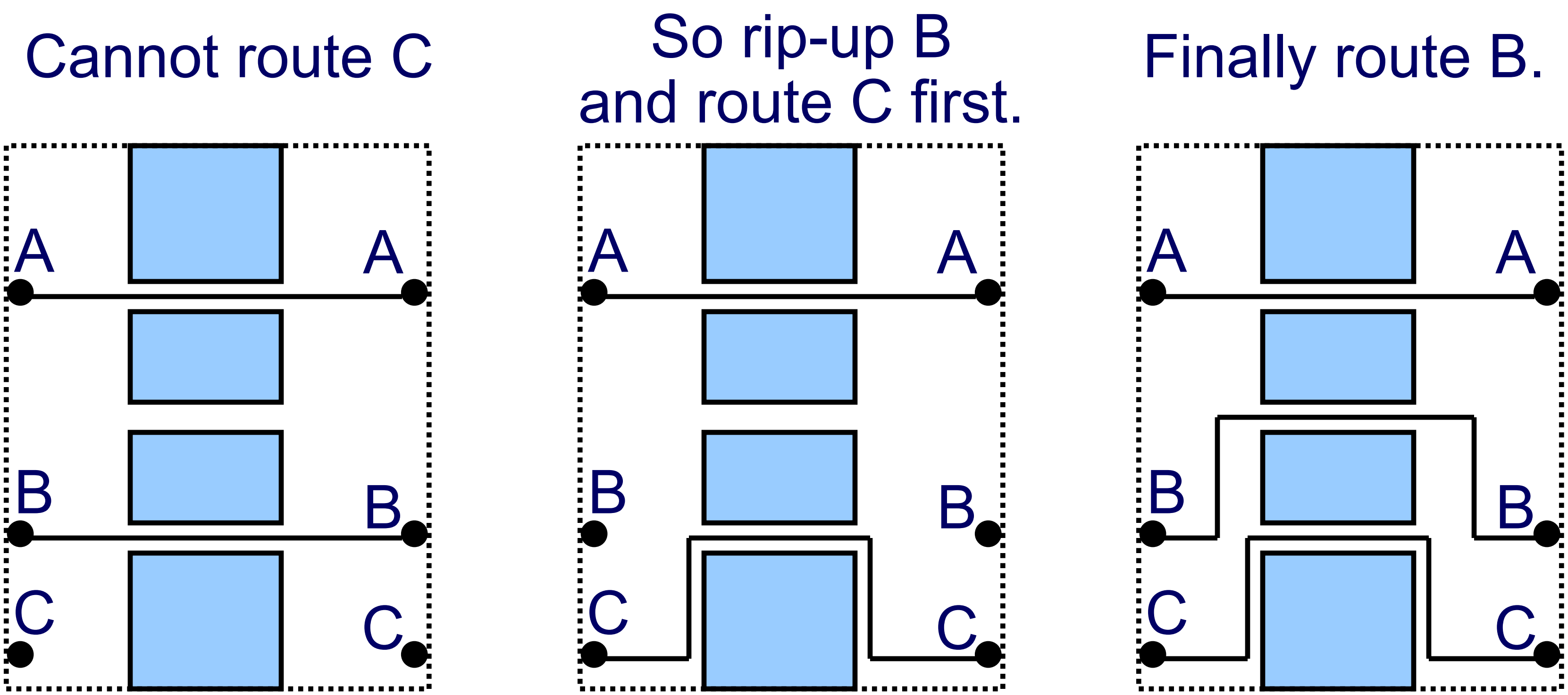


B first then A
(Good order)

A first then B
(Bad order)

- Length in placement
- Timing criticality
- Number of terminals

When a route for a net can't be found then rip up and re-route



[Example from Prof. D. Pan Lecture]

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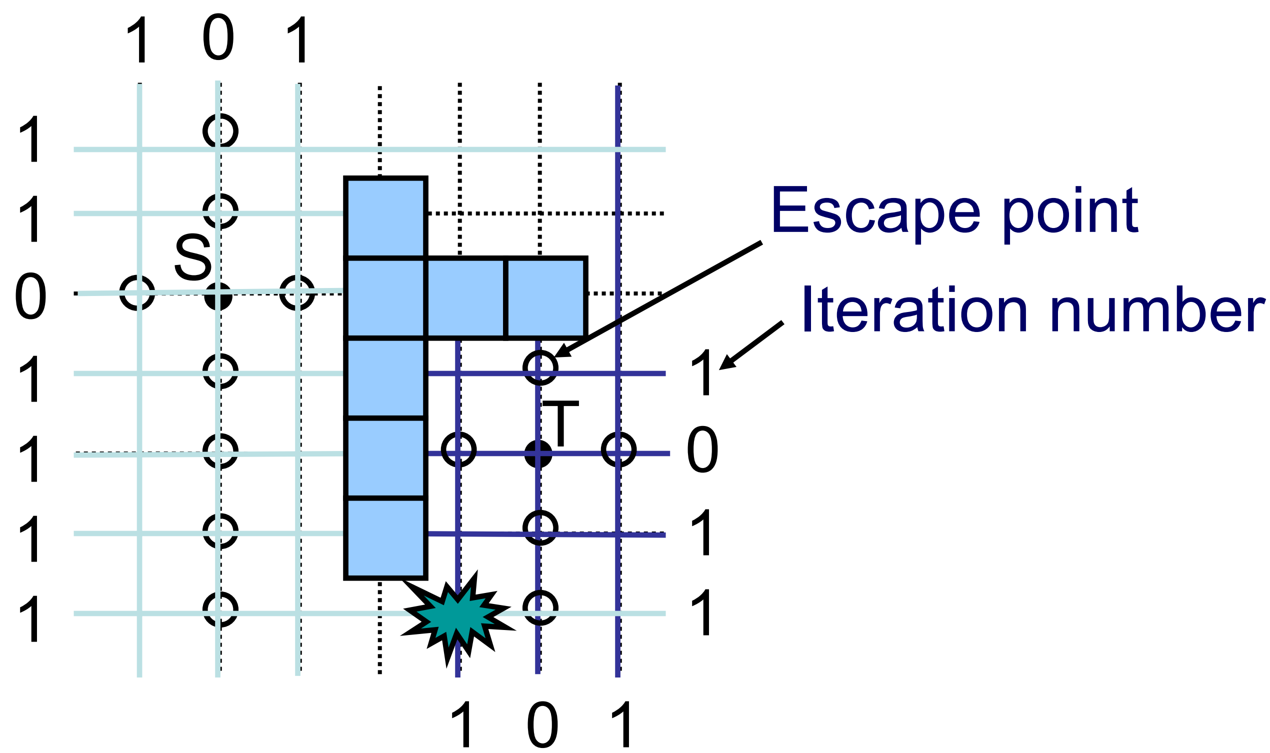
Line Probe Algorithm

- Each source (s) and destination (t) has their own set of segments
- Algorithm terminates when a line from the s set intersects with the t set



[animation sequence from Prof. D. Pan]

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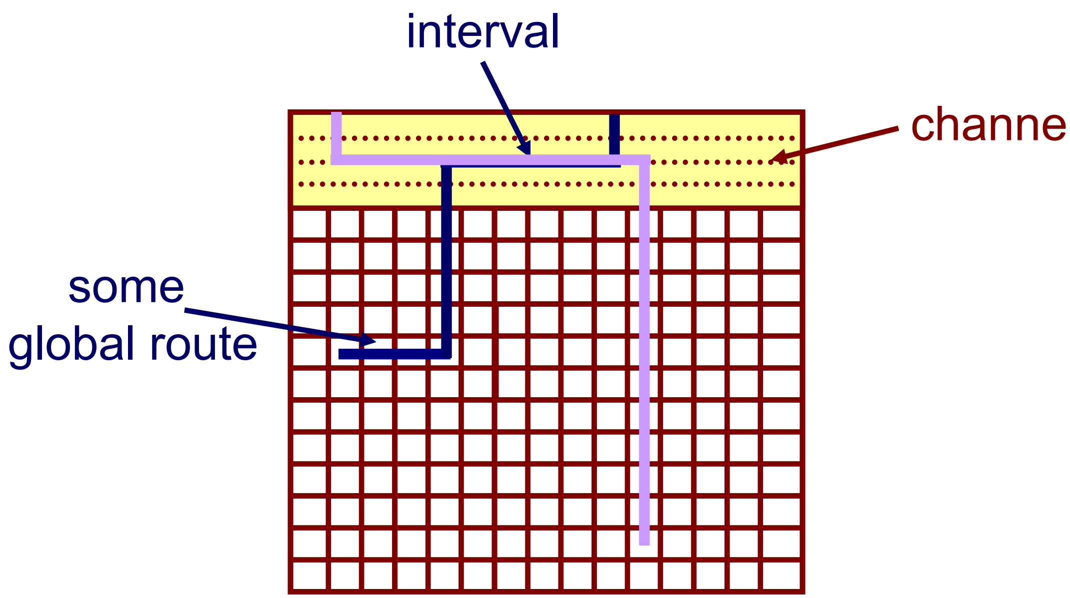
What happens after global routing?



- We need to assign exact tracks for each interval within a channel
- What criteria should our assignment technique use?
  - ➢ Intervals should fit within the available number of tracks
  - ➢ Cross talk minimization
  - ➢ Wirelength minimization (place intervals close to their pins in case all pins lie on one side of the channel
  - ➢ vias

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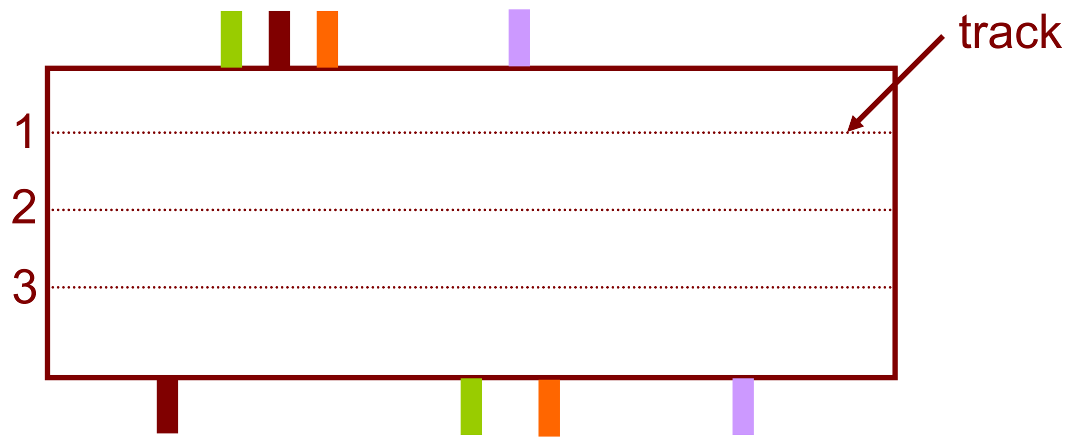
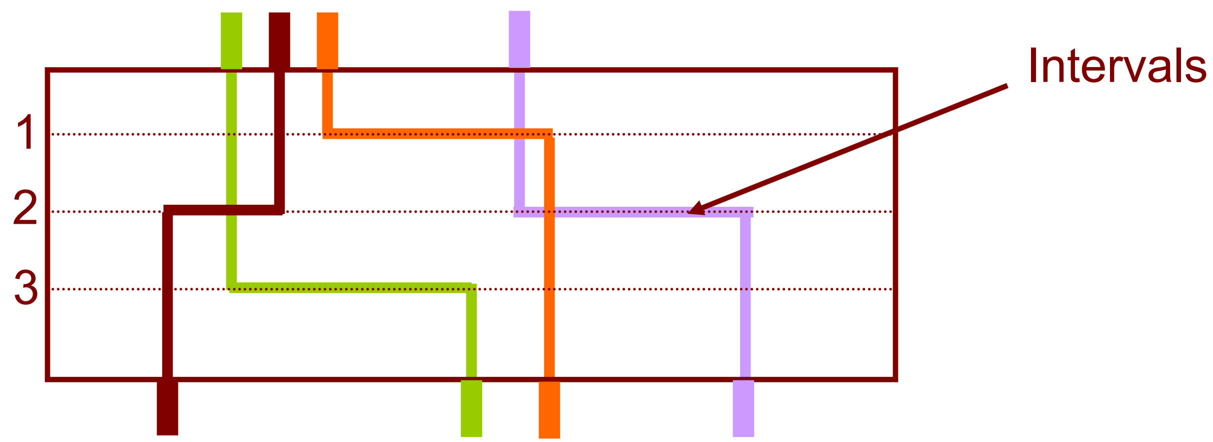
Left edge algorithm



Objective: Connect pins of the same colors using the minimum amount of tracks

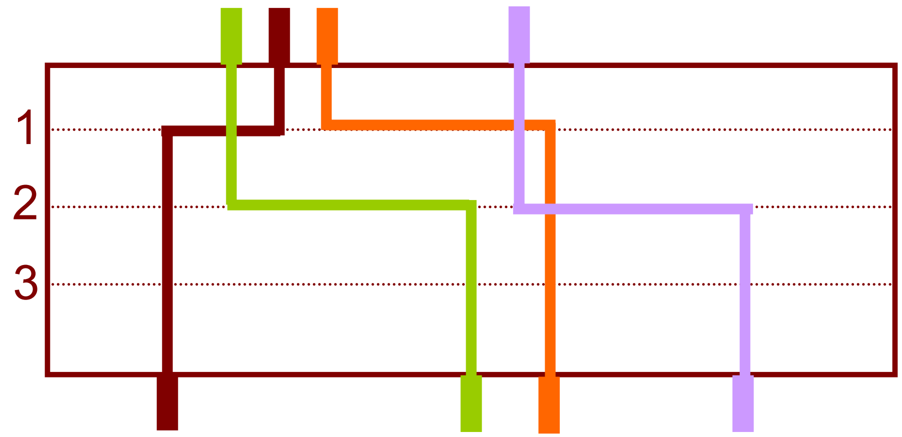
Let's try some random choices: Orange – Red – Violet - Green



Can we do better?

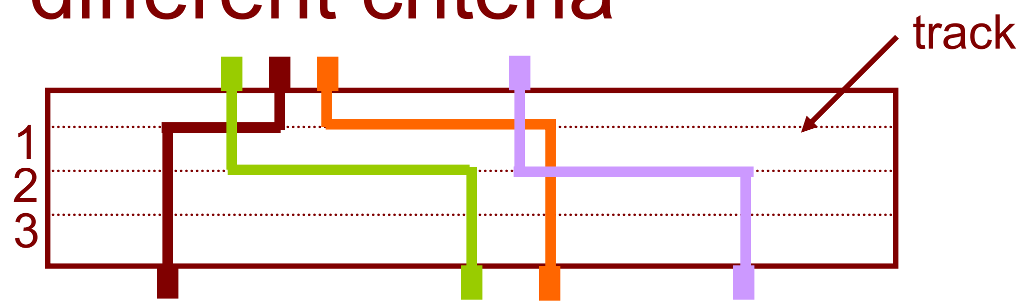
Left edge algorithm

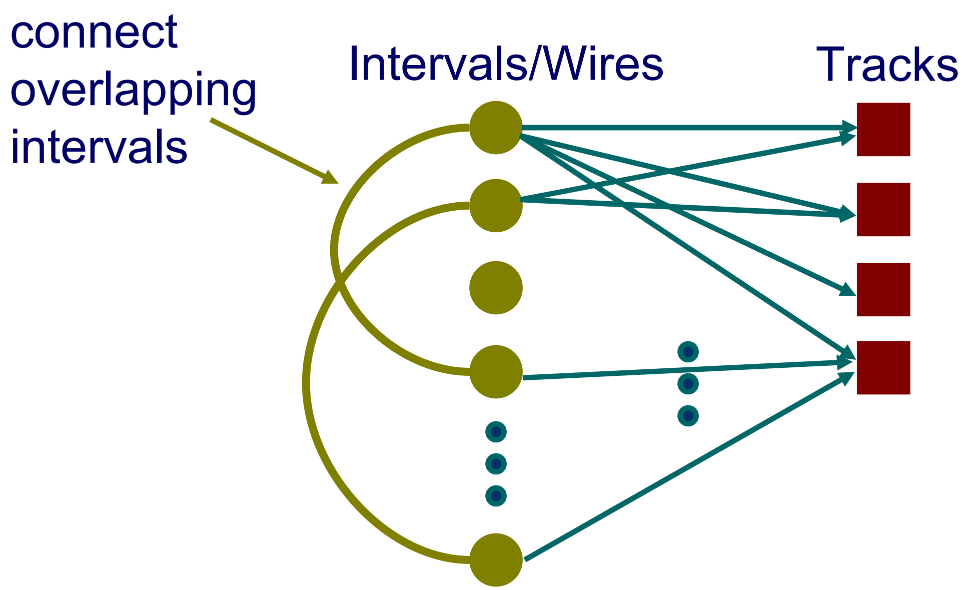
- Sort Intervals based on their location of their left edge
- For each interval in order:
  - Insert the interval in the first track that fits



We saved one track!
Why this algorithm always uses the minimum number of tracks?

In general, track assignment cost is a function of different criteria





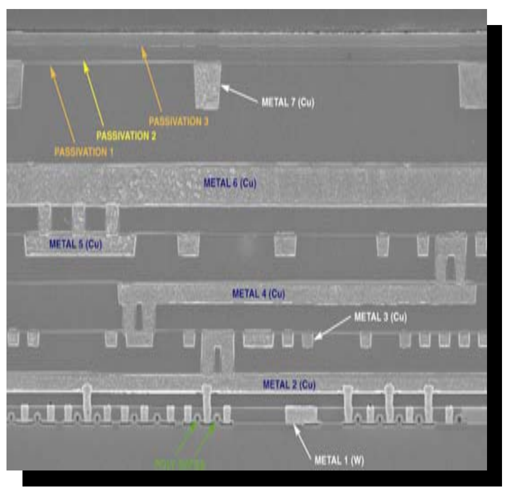
solution is in readings!

- Cost of assigning interval *i* to track *j* depends on wirelength / vias
- Find an assignment for each interval such that the total cost is minimized and such that no two overlapping intervals residing on the same track

Layer assignment

Criteria for layer assignments:

- The higher the metal layer, the larger the width/height of a wire → smaller resistance
- Metal layers have preferred direction (horizontal or vertical)
- Filling the lowest metal layers blocks vias from wires on higher metal layers
- Lower for local communication and higher layers for global communications
- Higher layers for signals that are timing critical



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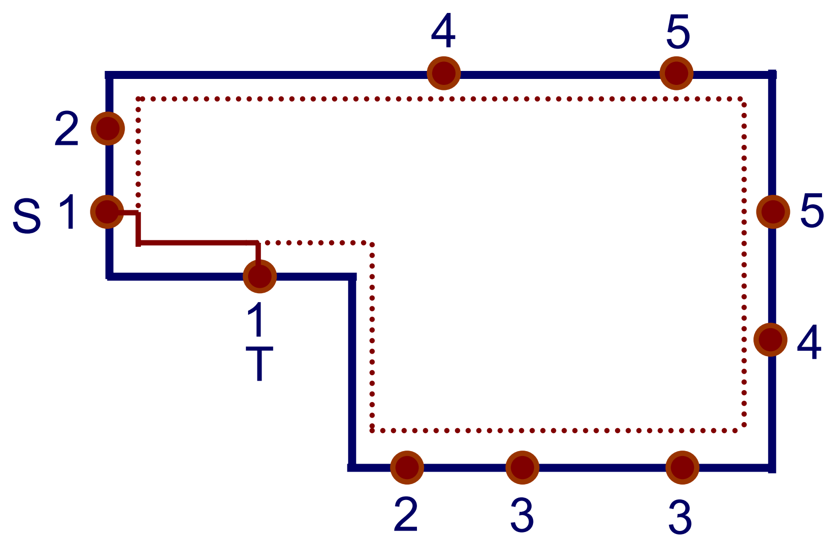
Special case: River routing

➢ Single layer routing → No two wires can intersect



- To connect two terminals, there are two possible paths
  - use the shortest of the two
- Traverse a path counter clock-wise and identify the source and the terminal nodes

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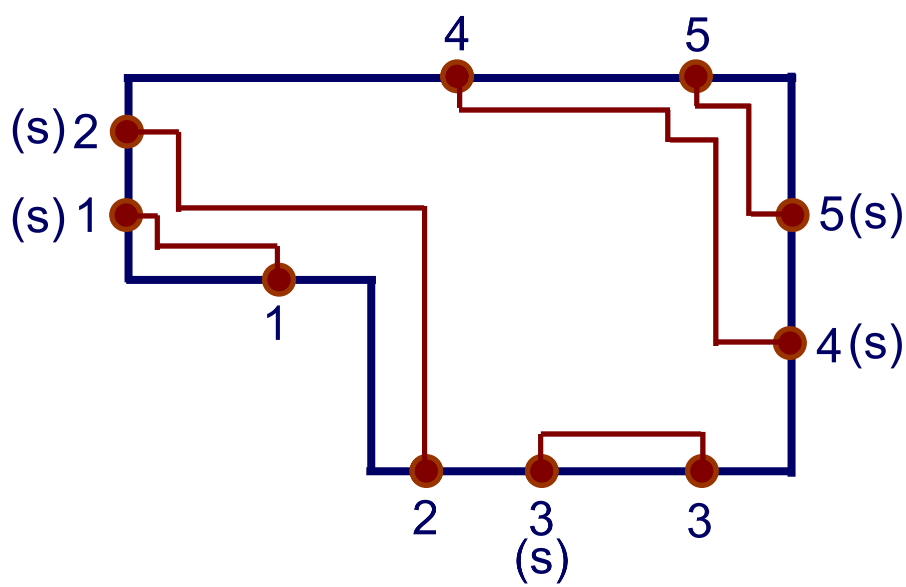
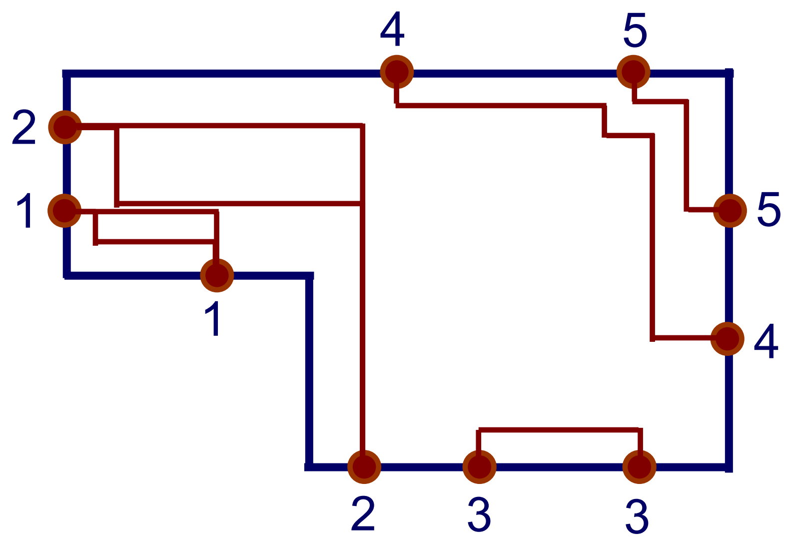
River routing: II. order the nets and route



- If a net *i* is contained within another net *j* then net *i* is routed before *j*.
  - Example: net 1 is contained within net 2
- Traverse the boundary in CCW matching end points to start points
- Whenever a net is routed it creates a pseudo boundary. Nets routed afterwards use the new boundary and are routed within minimum distance to the boundary

River Routing: III. Flip corners to minimize vias



- Start corner flipping from the outside to the inside
- Lot of (outdated) work on routers. We only covered the basics. Please consult the readings.

Assigned readings

- Track Assignment: A Desirable Intermediate Step Between Global Routing and Detailed Routing
- A Diagonal-Interconnect Architecture and Its Application to RISC Core Design
- BoxRouter: A New Global Router Based on Box Expansion and Progressive ILP

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Taxonomy of routers

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