Physical Design of Digital Integrated Circuits (EN0291 S40)

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Lecture 10: Repeater (Buffer) Insertion

- Introduction to Buffering
- Buffer Insertion
  - Two-pin nets
  - Multi-pin nets

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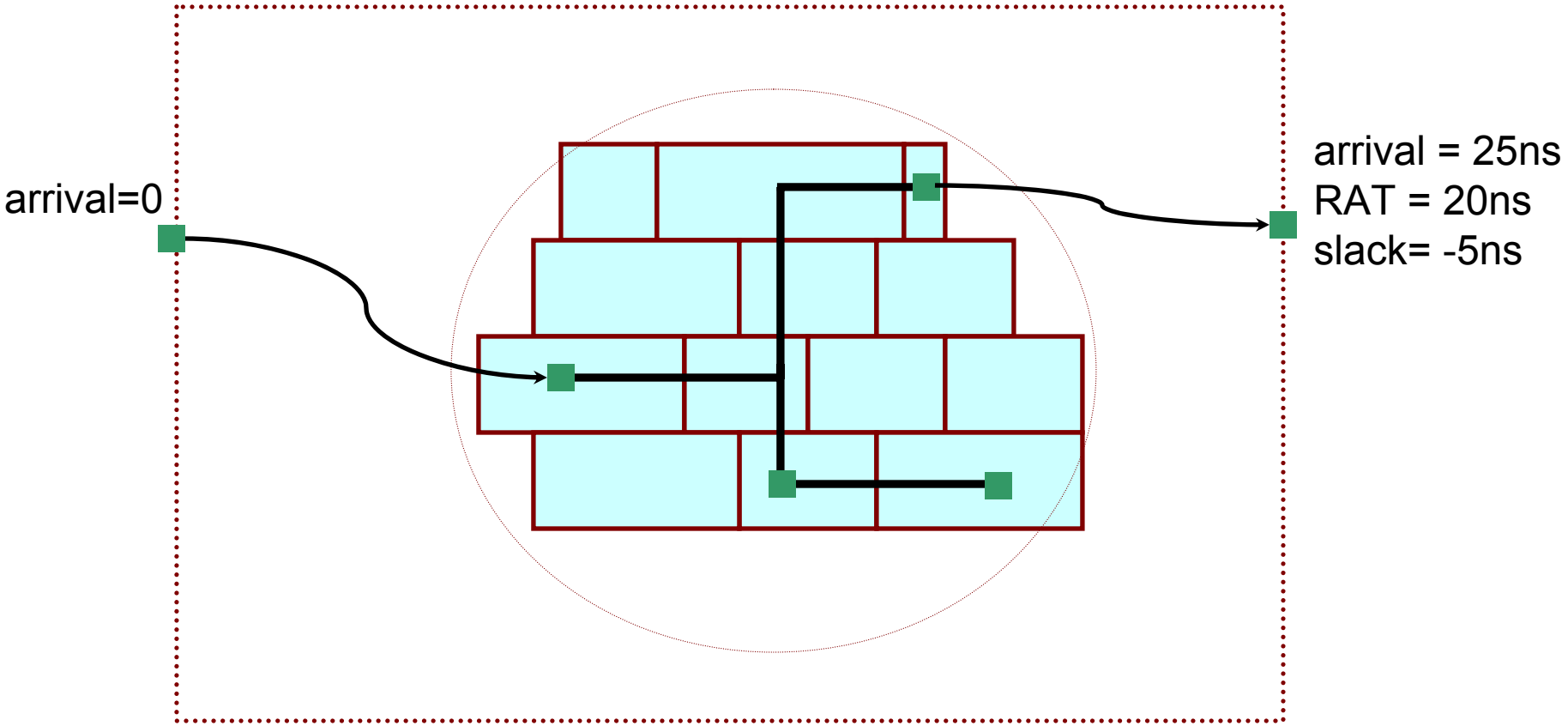
Big picture: when is buffering needed?



Placement → Steiner tree construction → STA
Timing is not met! What are you going to do?

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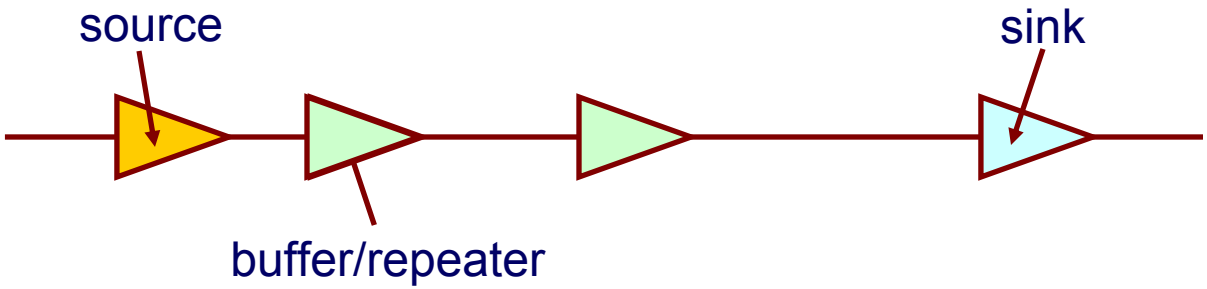
Buffer insertion in the simple case of two-pin wires



Q: How to improve the delay from source to sink? → Insert repeaters

Two questions:

- What is the position that minimizes the delay?
- How many repeaters to insert to minimize the delay?

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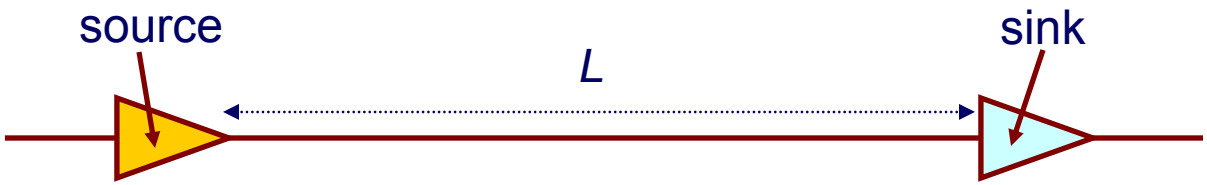
What is the delay from source to sink without any repeaters?



Delay from source to sink:

$D_0 = D_{src} + R_{src}(cL + C_{snk}) + rL(\frac{cL}{2} + C_{snk})$

D_{src}: intrinsic delay of source

R_{src}: effective output resistance

r/c: resistance/capacitance per unit length

L: wire length

C_{snk}: input capacitance of sink

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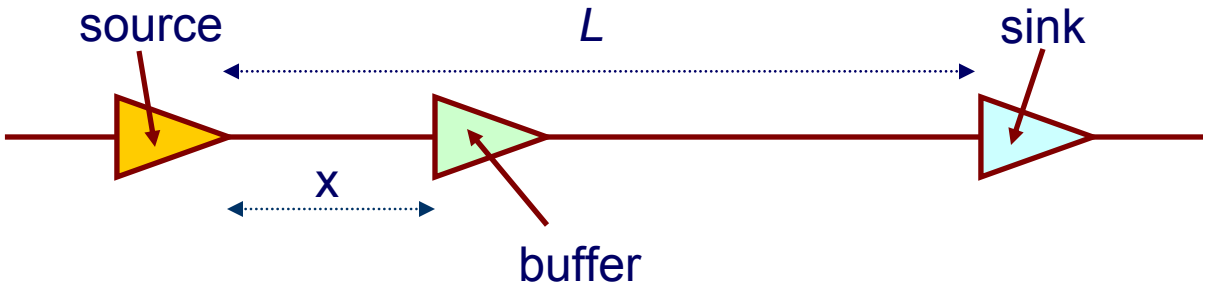
If you have one repeater, where is the optimal position to insert it?



Delay from source to sink:

$$D_1(x) = D_{src} + R_{src}(cx + C_{buf}) + rx(\frac{cx}{2} + C_{bf}) + D_{bf} + R_{bf}(c(L-x) + C_{snk}) + R(l-x)(\frac{c(l-x)}{2} + C_{snk})$$

Minimum delay is attained when

$$\frac{dD_1(x)}{dx} = 0 \text{ at } x = \frac{L}{2} + \frac{R_{buf} - R_{snk}}{2r} + \frac{C_{snk} - C_{buf}}{2c}$$

Makes sense to add a buffer only if D_0-D_1 > 0

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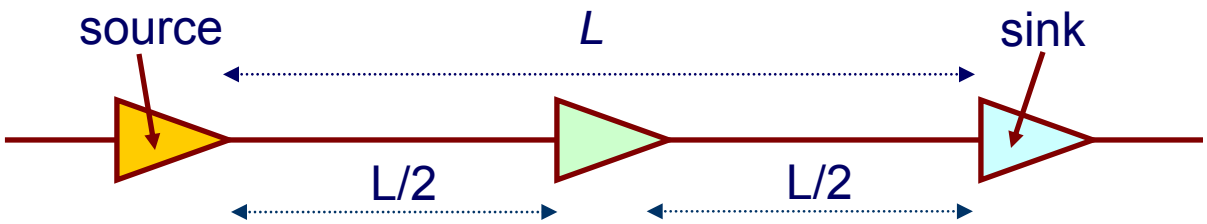
If there are multiple buffers, where are the optimal locations to insert them?



$$\frac{dD_1(x)}{dx} = 0 \text{ at } x = \frac{L}{2} + \frac{R_{buf} - R_{snk}}{2r} + \frac{C_{snk} - C_{buf}}{2c}$$

If $R_{buf} = R_{snk}$ and $C_{snk} = C_{buf}$
then the optimal location for the buffer is at distance L/2

If there are *k* buffers then minimum delay will occur when they are equally spaced, i.e., separation distance is *L/(k+1)*

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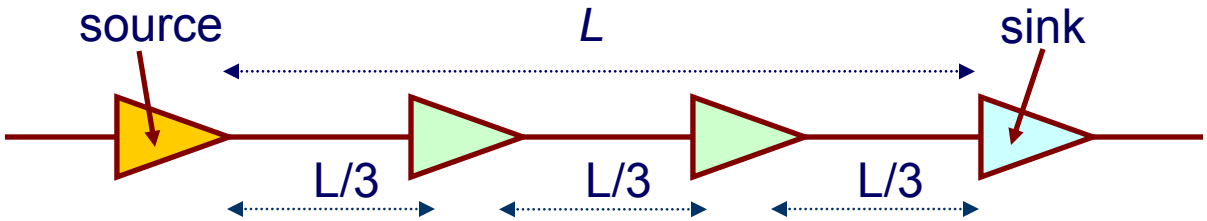
How many repeaters can we keep adding to minimize the delay?



Same analysis as before!

Delay from source to sink:

$$D_2(x) = D_{src} + R_{src}(\frac{cL}{3} + C_{buf}) + \frac{rL}{3}(\frac{cL}{6} + C_{bf})$$
$$+ D_{bf} + R_{bf}((\frac{cL}{3} + C_{bf}) + \frac{RL}{3}(\frac{cL}{6} + C_{bf})$$
$$+ D_{bf} + R_{bf}(\frac{cL}{3} + C_{snk}) + \frac{RL}{3}(\frac{cL}{6} + C_{snk})$$

If $D_2 < D_1$ then use two buffers

Keep on adding buffers until $D_{k+1} \geq D_k$ then the optimal number of buffers is k (see lecture readings for a closed form of k)

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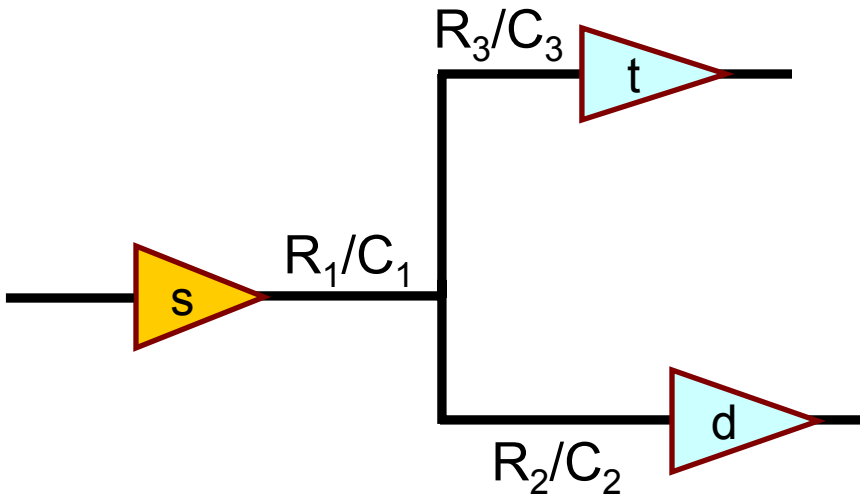
Recap: How to calculate pin-to-pin delay in multi-pin trees?



Delay from $s \rightarrow t$:

$$D_s + R_s(C_1 + C_3 + C_2 + C_t + C_d)$$
$$+R_1(C_1/2+C_2+C_3+C_t+C_d)+R_3(C_3/2+C_t)$$

Delay from $s \rightarrow t$:

$$D_s + R_s(C_1 + C_3 + C_2 + C_t + C_d)$$
$$+R_1(C_1/2+C_2+C_3+C_t+C_d)+R_2(C_2/2+C_d)$$

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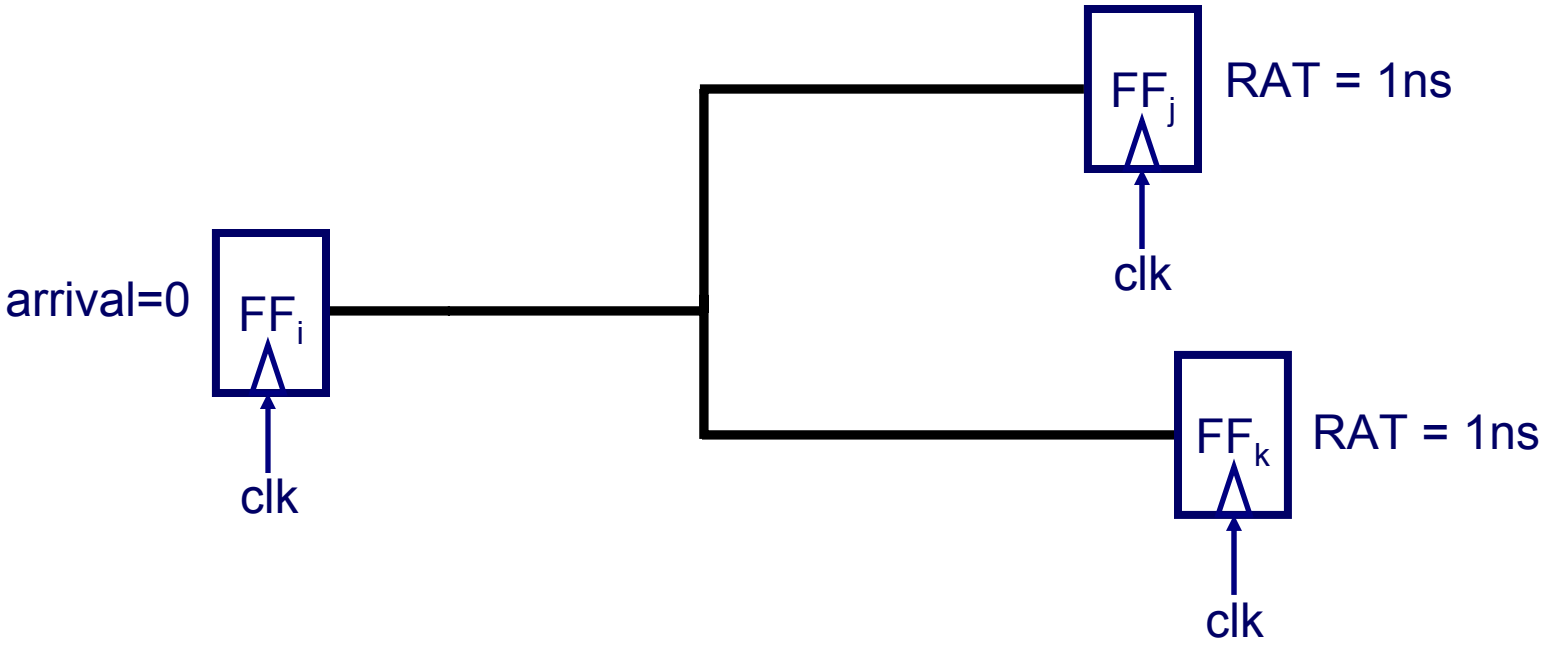
Repeater insertion in trees



Suppose this is a simple circuit that is required to operate at 1GHz

Assume the delay from i to j is 1.1ns and the delay from i to k is 1.2ns
Therefore the slack at the source is min(1-1.2, 1-1.1) = -0.2

Our objective is to maximize the slack at the source (hint: minimize the delay from source to sinks via repeater insertion)

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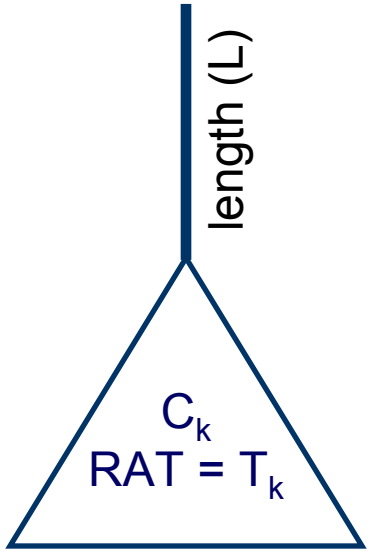
Basic operations: adding a wire

$$\text{load} = C_k + cL$$

$$\text{slack} = T_k - rLC_k - \frac{rcL^2}{2}$$



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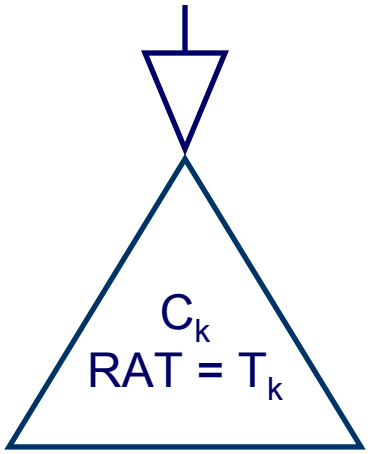
Basic operations: adding a buffer

$$\text{load} = C_{buf}$$
$$\text{slack} = T_k - RC_k - D_{buf}$$



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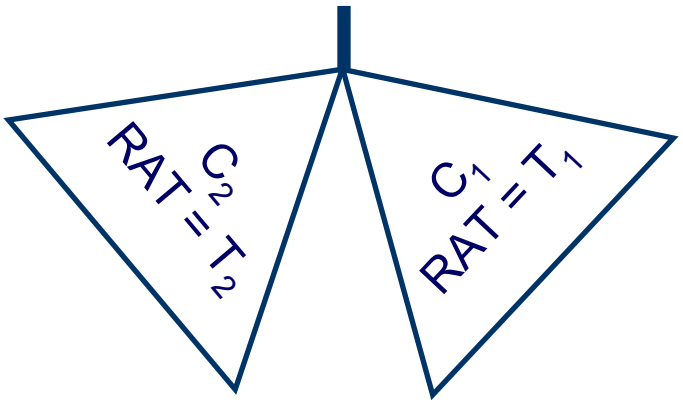
Basic operations: merging two subtrees

$$\text{load} = C_1 + C_2$$
$$\text{slack} = min(T_1, T_2)$$



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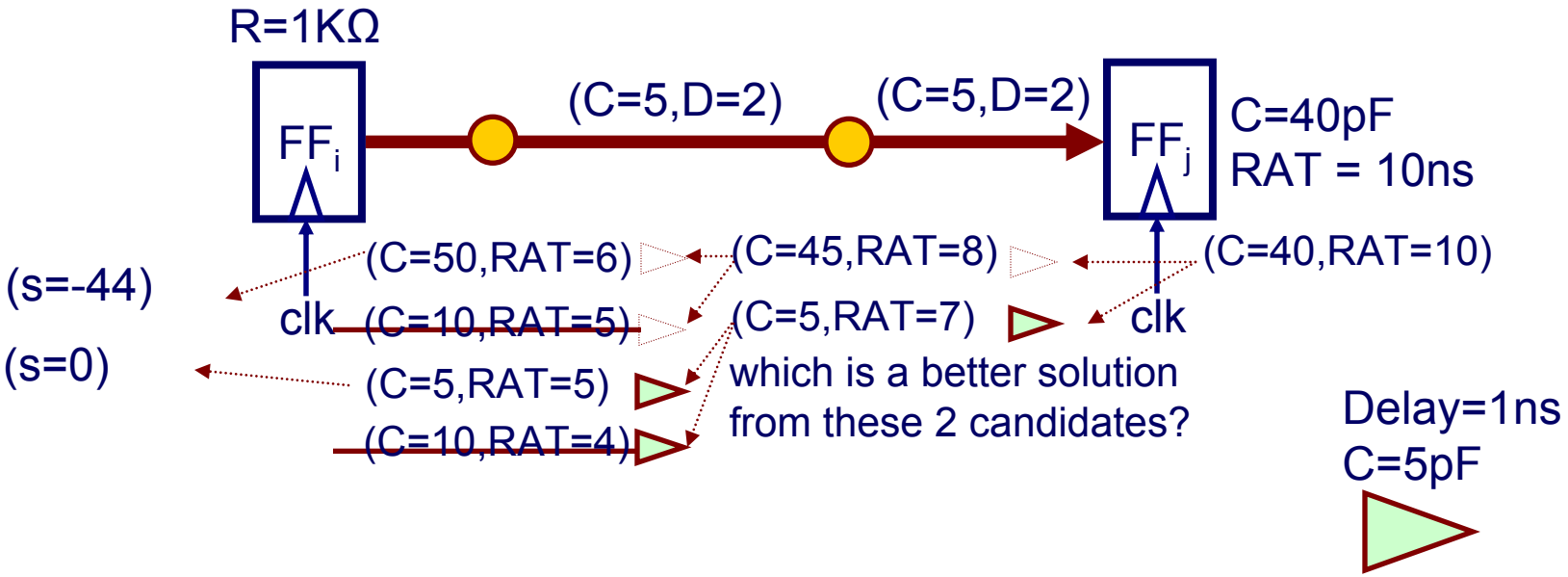
Generating candidates: the buffer case

R: Effective output resistance,
C: capacitance (input pin/wire)
RAT: Required Arrival Time for the circuit to work according specifications
D: delay



Rule (C_2, R_2) is considered redundant candidate if
There exists some other candidate (C_1, R_1) such R1 ≥ R2 and C1 ≤ C2

→ Adding a buffer can only increase the candidate list size by 1

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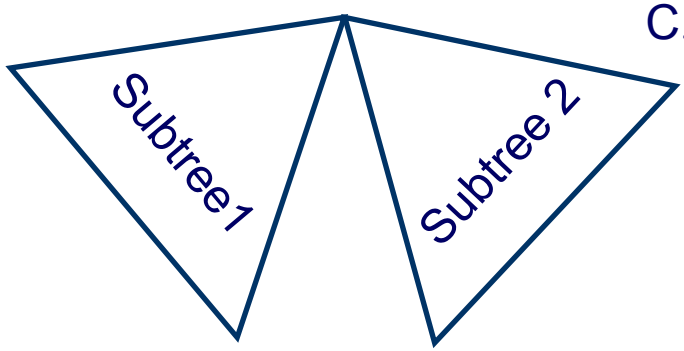
Generating candidates: the merging case

Candidates of subtree 1

(C_{11}, RAT_{11})
(C_{21}, RAT_{21})
$(C.., RAT..)$
(C_{n1}, RAT_{n1})
$RAT_{11} > RAT_{21} > .. > RAT_{n1}$
$C_{11} < C_{21} < \ldots < C_{2n}$

Candidates of subtree 2

(C_{12}, RAT_{12})
(C_{22}, RAT_{22})
$(C.., RAT..)$
(C_{m2}, RAT_{m2})
$RAT_{12} > RAT_{22} > .. > RAT_{m2}$
$C_{12} < C_{22} < \ldots < C_{m2}$



What is the maximum number of candidates in the newly merged subtree?

At most n+m. For every RAT value, we only need to keep the candidate with the least capacitance!

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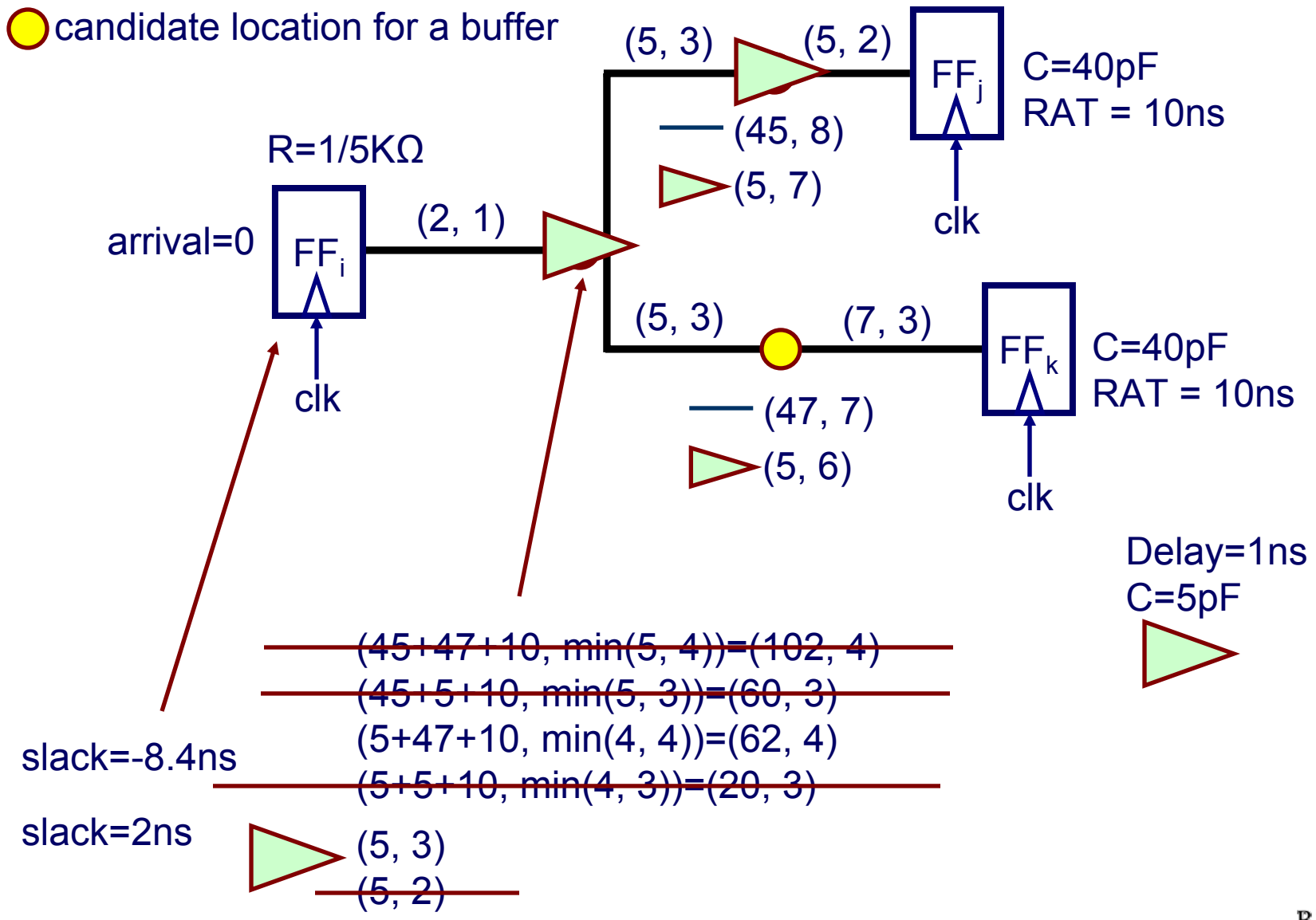
Van Ginneken algorithm



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Van Ginneken algorithm summary

- Bottom-up pass: calculate the various candidate solutions
- Top-down pass: select the winning solution
- Complexity?

More questions

- How to minimize the number of buffers?
- How to determine simultaneously the tree topology and the buffers required?
- How to use inverters as well as buffers in repeater insertion?
- How to size a buffer?
- How to simultaneously size buffers and wires?
- ……
- Please check recommended readings

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Assigned Readings

- Optimal Wire Sizing and Buffer Insertion for Low Power and a Generalized Delay Model, DAC'95
- Interconnect Layout Optimization by Simultaneous Steiner Tree Construction and Buffer Insertion, ICCAD'96
- Minimum-Buffered Routing of Non-Critical Nets for Slew Rate and Reliability Control, ICCAD'01