BROWN UNIVERSITY

Dream Team 1

The calculator of your dreams

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I. Overall Design Specification

This document describes the design of a simple 16-bit calculator with a matrix-keyboard input and an external 7-segment display output. This calculator design supports addition, subtraction, multiplication, and accumulation. Results are latched into output registers and displayed externally on four 7-segment displays. All keypad interfacing and output logic is performed on the IC. A high level block diagram is shown in Figure 1.

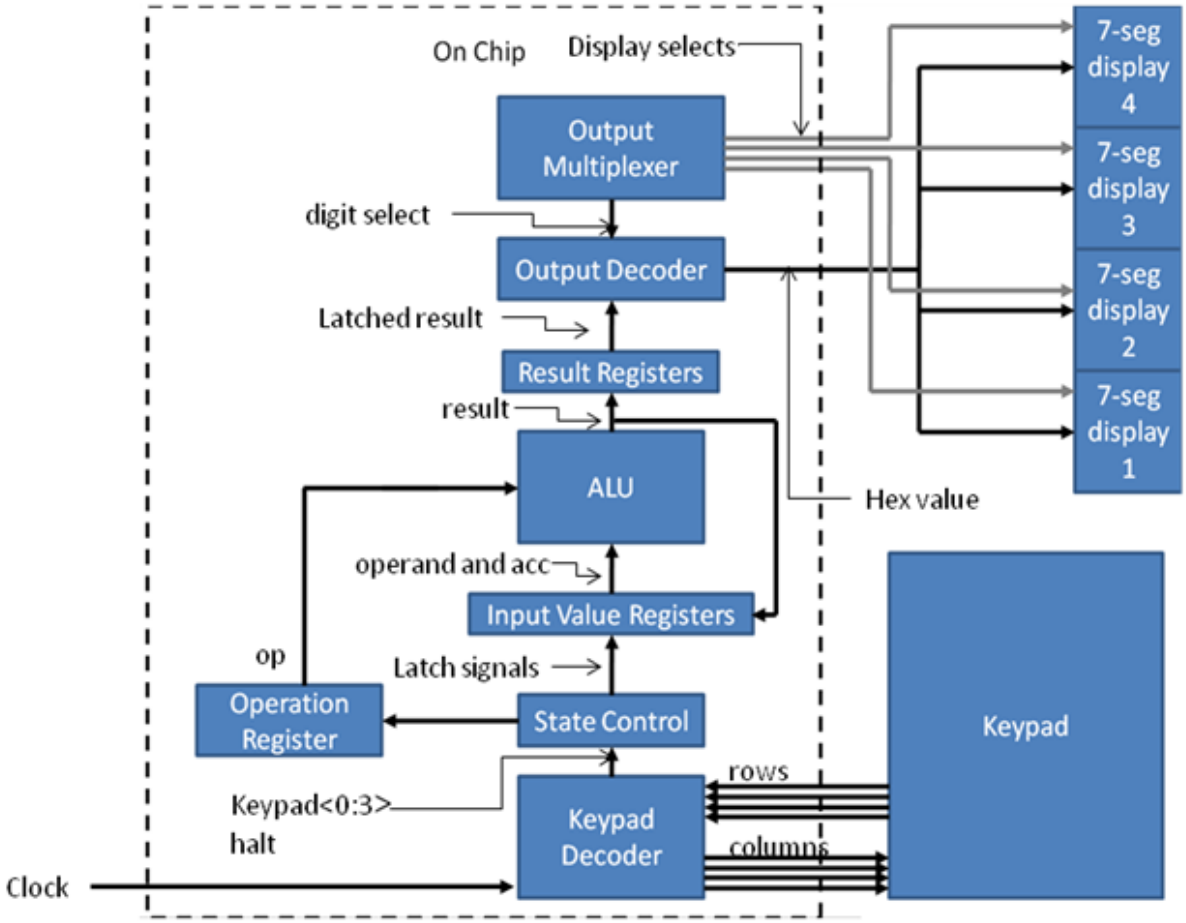


Figure 1 High level block diagram of calculator design

II. Block Diagram Description

Keypad Decoder – This block continuously scans the keypad using the input/output ports. When a key is pressed, it connects the input signal from a column to the output on a certain row. By decoding these row-column combinations the output can be determined.

Inputs are the rows of the matrix keypad and the clock.

Outputs are the column strobe signals as well as the value decoded from the button press and the type of the key press recorded. A halt signal is also asserted for as long as a key press is recognized.

State Control – This block regulates the entire system as it determines data's path through the different logic blocks of the calculator. It selects which register will receive the value output by the keypad decoder, which operation the ALU should perform, and what will be displayed along the way. The state is kept track of internally in six registers using a one-hot encoding scheme.

Inputs for this block consist of the type of input determined by the keypad decoder and the halt signal from the keypad decoder.

Outputs are the control signals for all the multiplexers as well as latch signals for the registers.

ALU – This block performs the arithmetic operation specified by the operation register. Two control signals distinguish between addition, subtraction and multiplication. A multiplexer is used to connect the output to the correct value and it is stored in a register to be displayed.

Inputs consist of two operands and two control signals

Output is the result of the calculation which is stored in a register.

Output Decoder – This block maps the binary value in each of the 4-bit result registers into a hexadecimal character on its corresponding 7-segment display.

Inputs are the four 4-bit values to be displayed and the clock.

The output is the seven-segment representation of one four-bit number.

Output Multiplexer – This block continuously cycles through the four 7-segment displays and selects a digit to illuminate based on a decoded two-bit counter. In order to reduce the number of I/O pins required the displays are

multiplexed. This reduces the number of required output lines from twenty-eight to eleven. Of the eleven pins, seven are for the seven segment display control and the other four are select lines for the pins.

Inputs are the clock and the four four-bit numbers to display

Outputs are one four-bit number and a select signal.

III. System Design

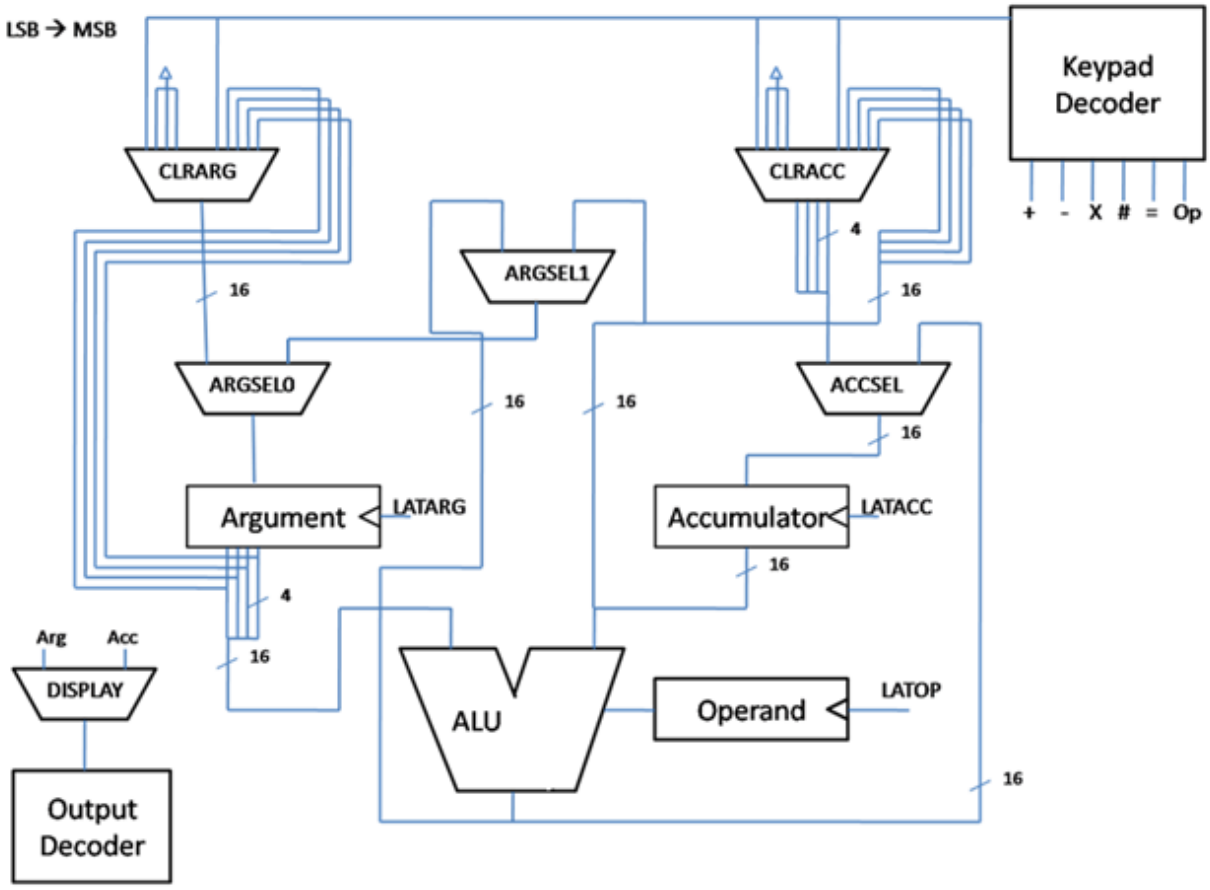


Figure 2 An overview of the system design

IV. I/O Description

Table 1 Pin-out descriptions

Pin Location	I/O Type	Name	Description
L6	Input	CLK	Clock signal.
R4	Output	C3	Connects to column 3 of keypad matrix.
R3	Output	C2	Connects to column 2 of keypad matrix.
R2	Output	C1	Connects to column 1 of keypad matrix.
R1	Output	C0	Connects to column 0 of keypad matrix.
L5	Input	R4	Connects to row 4 of keypad matrix.
L4	Input	R3	Connects to row 3 of keypad matrix.
L3	Input	R2	Connects to row 2 of keypad matrix.
L2	Input	R1	Connects to row 1 of keypad matrix.
L1	Input	R0	Connects to row 0 of keypad matrix.
T1	Output	SEGA	Connects to segment A of selected 7-segment display.
T2	Output	SEGB	Connects to segment B of selected 7-segment display.
T3	Output	SEGC	Connects to segment C of selected 7-segment display.
T4	Output	SEGD	Connects to segment D of selected 7-segment display.
T5	Output	SEGE	Connects to segment E of selected 7-segment display.
T6	Output	SEGF	Connects to segment F of selected 7-segment display.
T7	Output	SEGG	Connects to segment G of selected 7-segment display.
R8	Output	SEL3	Selects 7-segment display 3.
R7	Output	SEL2	Selects 7-segment display 2.
R6	Output	SEL1	Selects 7-segment display 1.
R5	Output	SEL0	Selects 7-segment display 0.
L10	--	VDD	3.3 V
R10	--	GND	Ground pin.
B1	Output	ALU15	Bit 15 off of ALU.
B2	Output	ALU14	Bit 14 off of ALU.
B3	Output	ALU13	Bit 13 off of ALU.
B4	Output	ALU12	Bit 12 off of ALU.
B5	Output	ALU11	Bit 11 off of ALU.
B6	Output	ALU10	Bit 10 off of ALU.
B7	Output	ALU9	Bit 9 off of ALU.
B8	Output	ALU8	Bit 8 off of ALU.
B9	Output	ALU7	Bit 7 off of ALU.
B10	Output	ALU6	Bit 6 off of ALU.

(L = Left, R = Right, T = Top, B = Bottom)

V. Task allocation

The various components were divided amongst the team members as follows:

Adder - Caitlin

Multiplier - Aung

Keypad decoder - Ryan

Control – Ryan, Aaron

Output/Display- Aaron

System assembly – Caitlin

VI. State Diagram

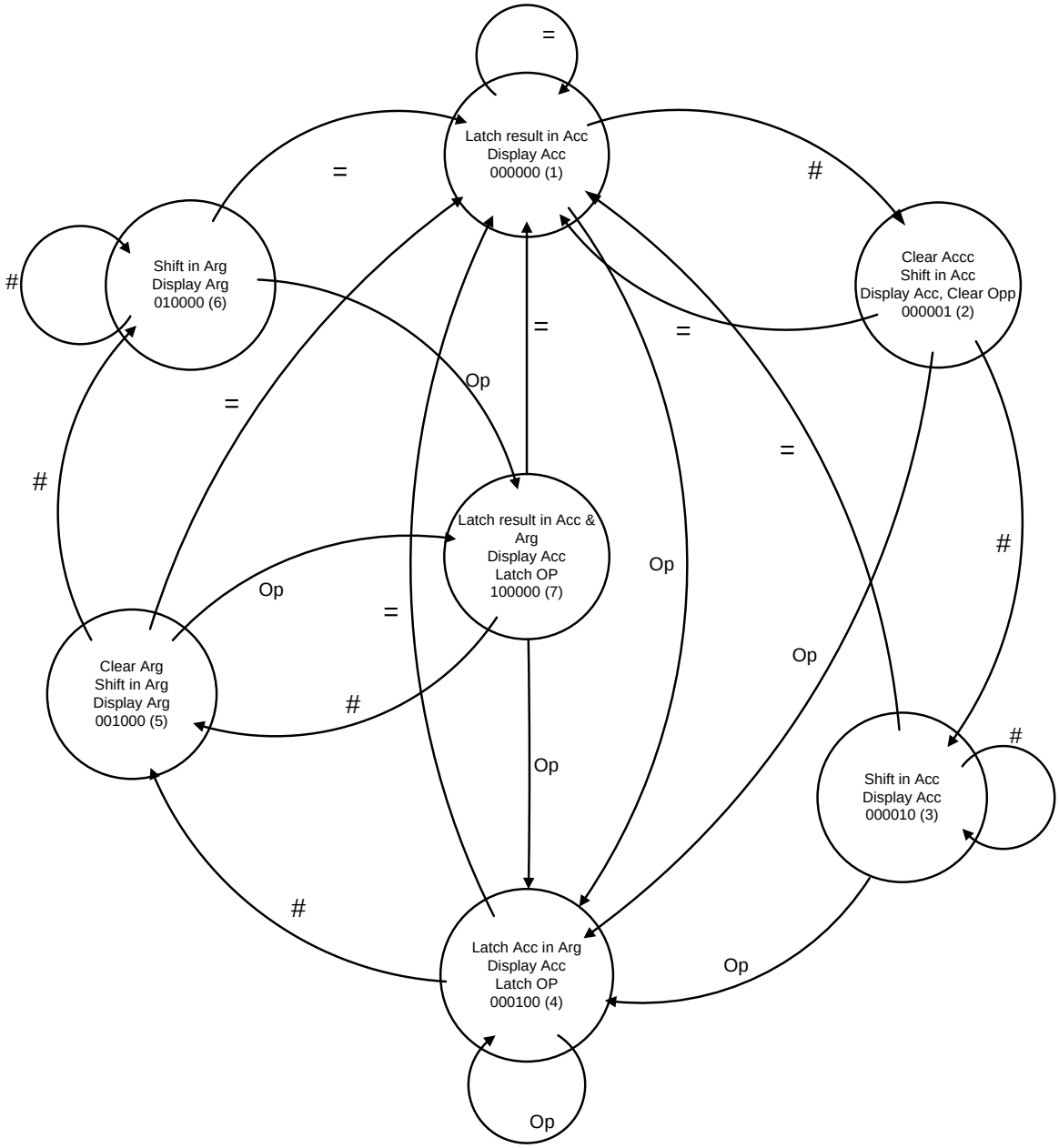


Figure 3 Finite state machine that supports all possible input combinations

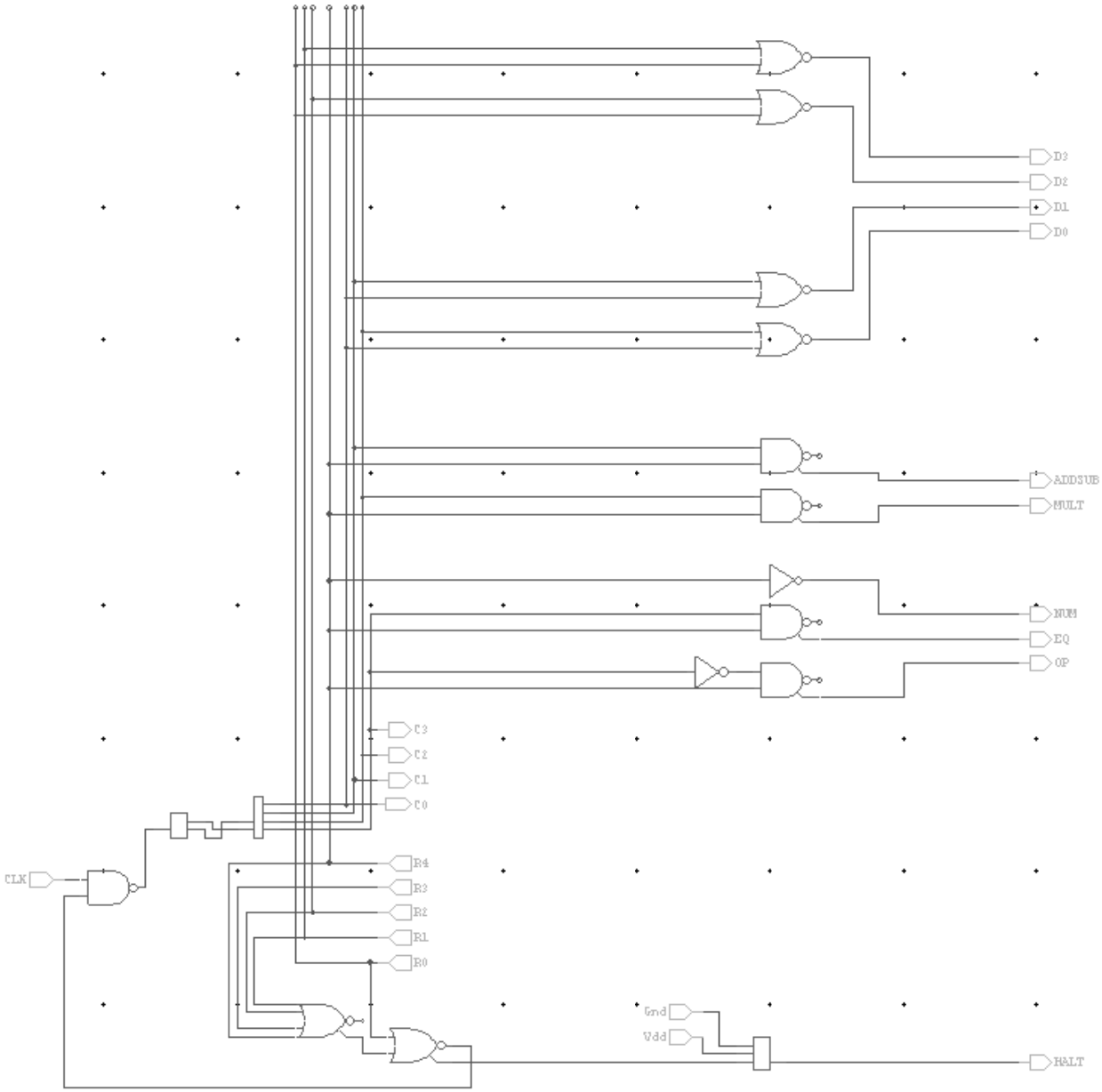
VII. Main Component Sizes

Table 2 Main component sizes

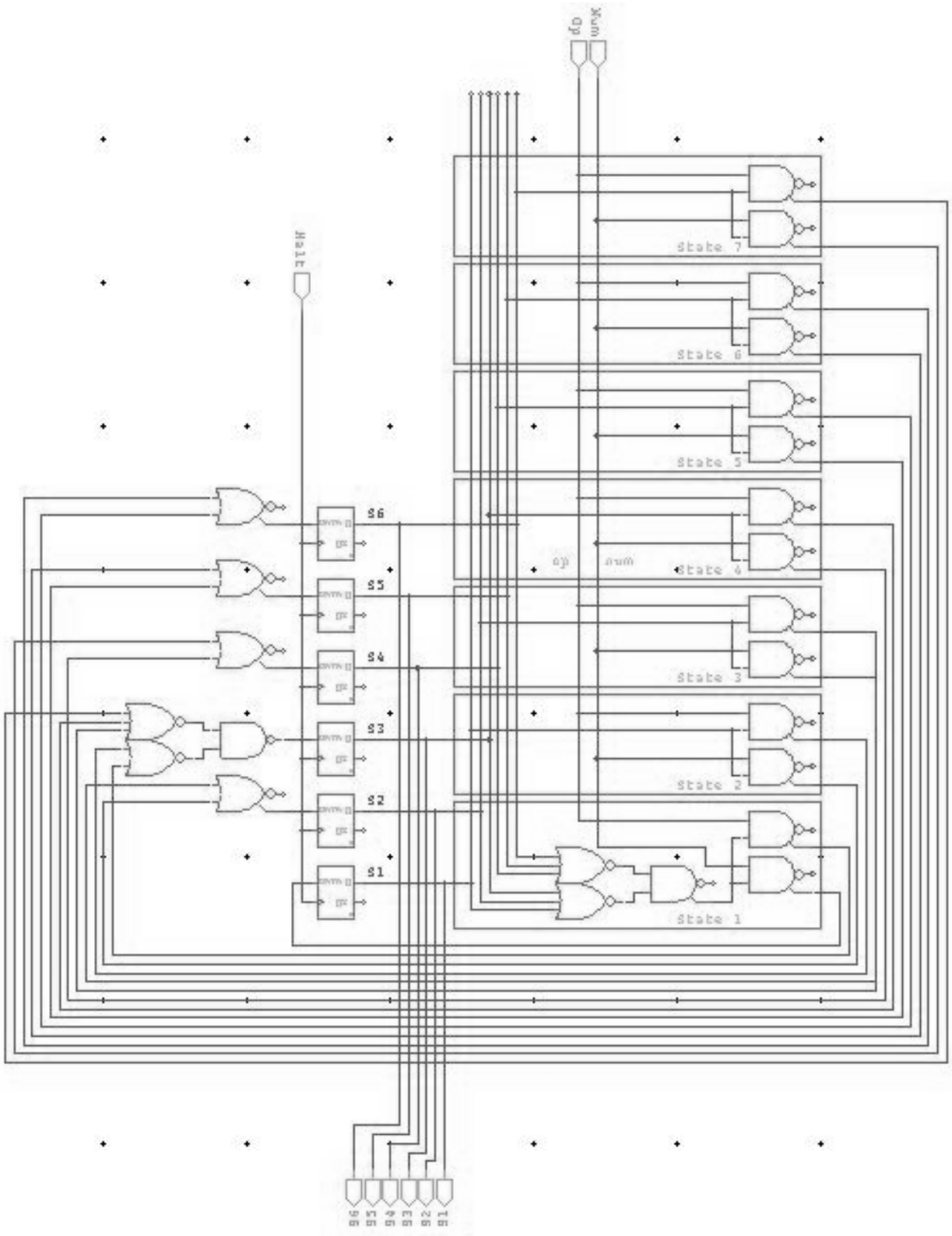
Component	Number of Standard Cells	Signals in Netlist	Core size dim 1 (λ)	Core size dim 2 (λ)	Area (λ^2)
Keypad Decoder	29	46	403.5	410.0	165435
Adder	128	161	808.0	775.5	626604.0
Multiplier	224	312	1389.0	545.0	757005.0
Output Decoder	82	102	605.0	940.5	569002.5
System Assembly	461	604	2226.5	1992.5	4436301.3

VIII. Schematics

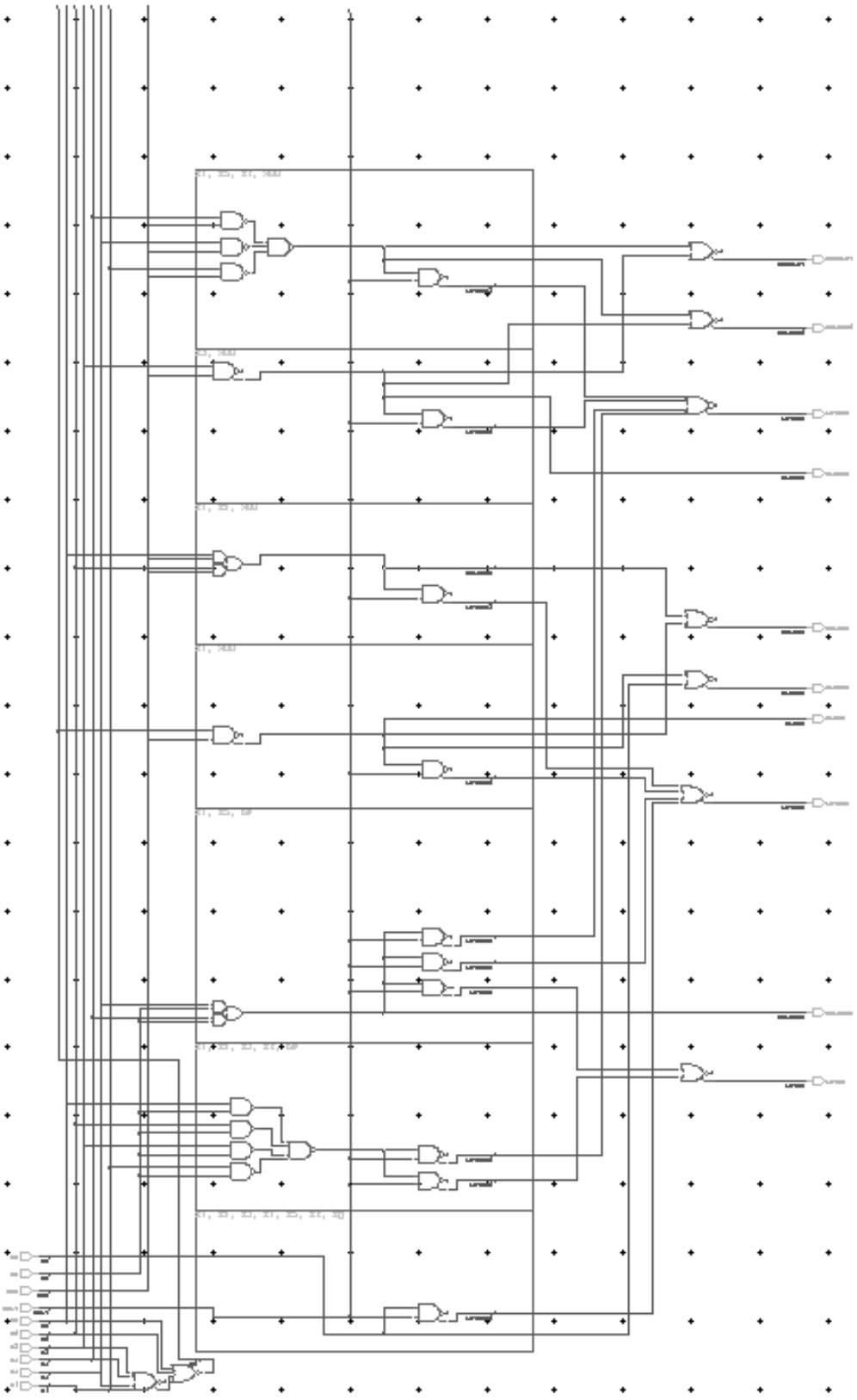
Keypad Decoder



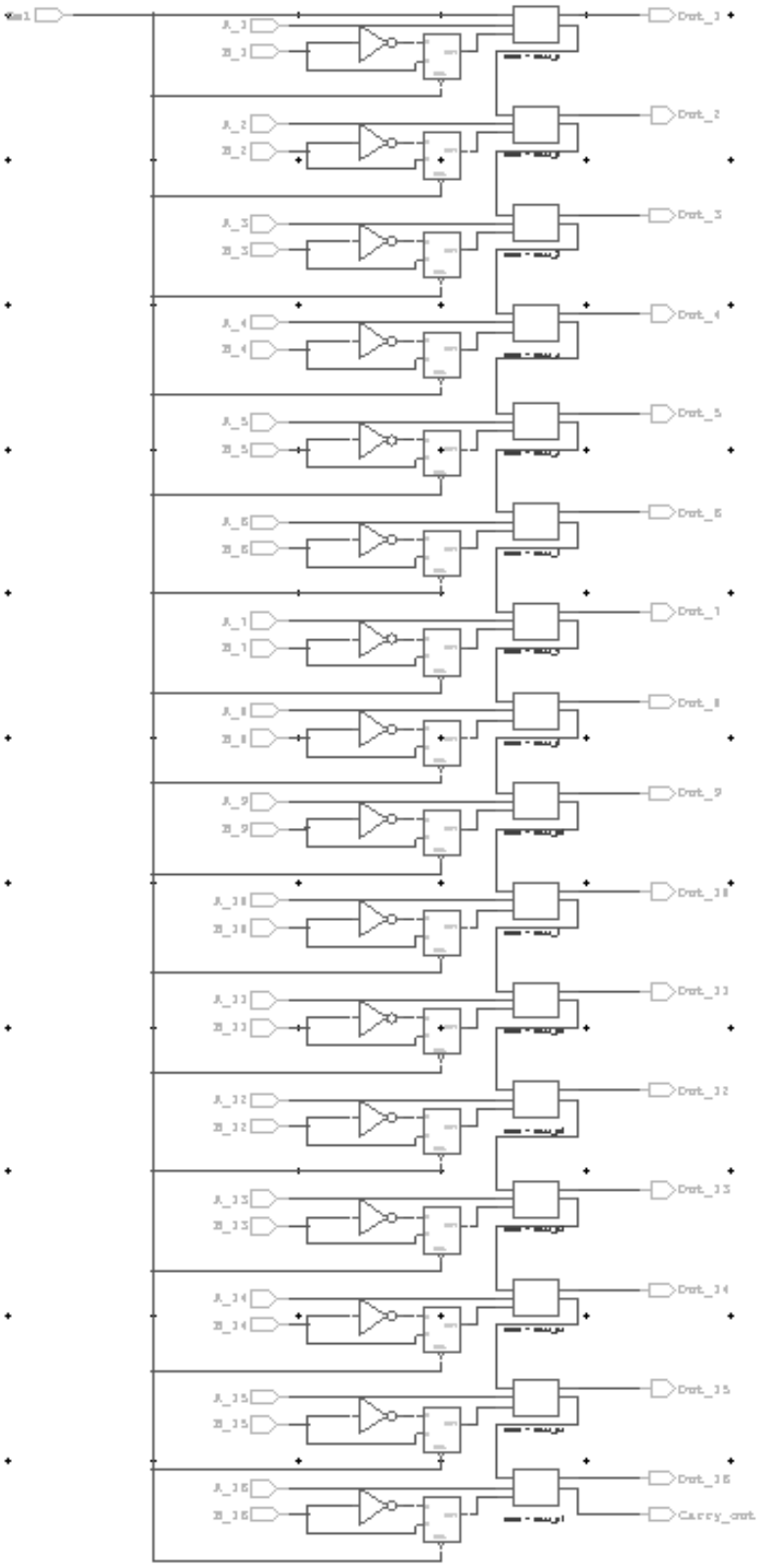
State Controller



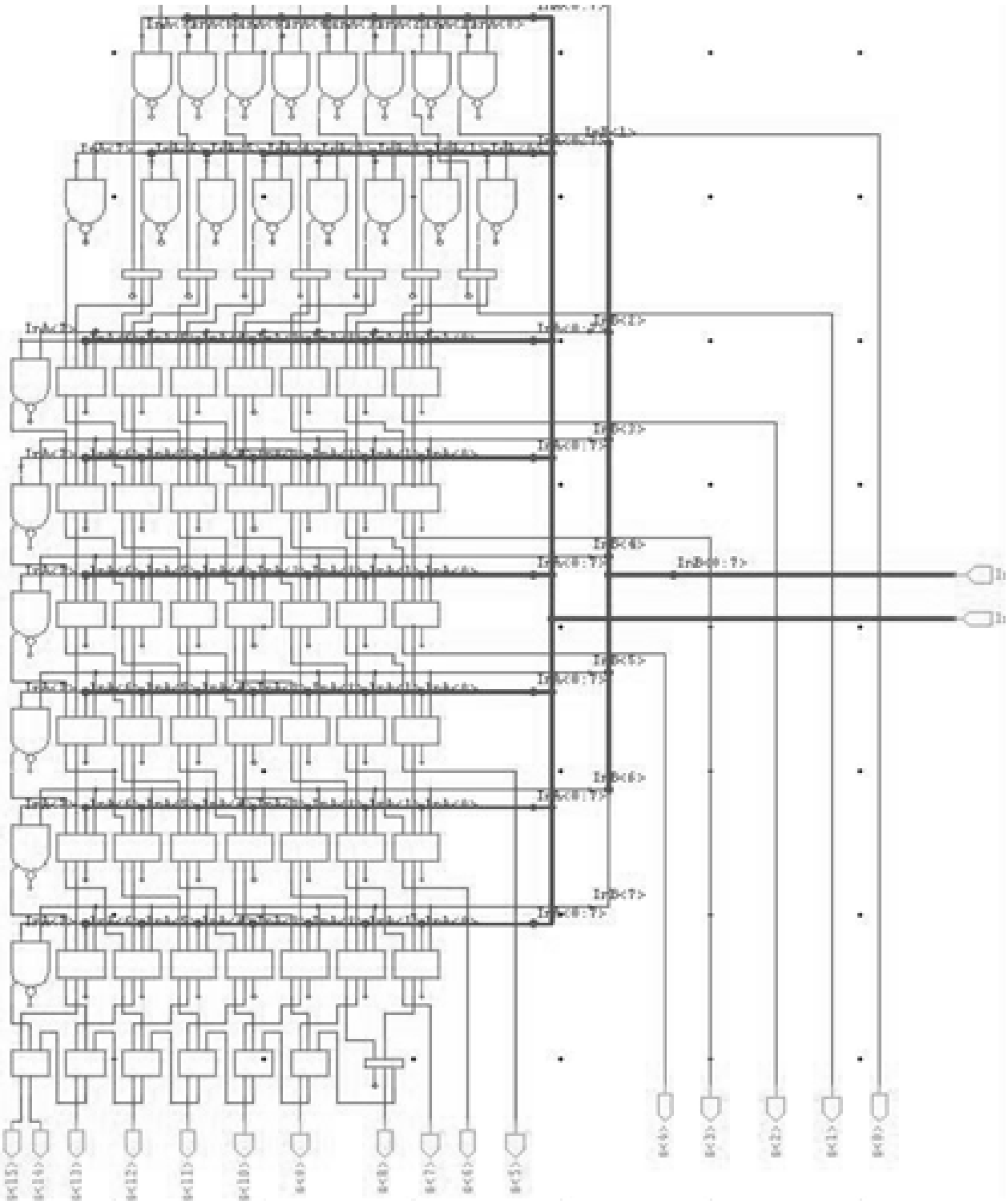
Control Signal Decoder



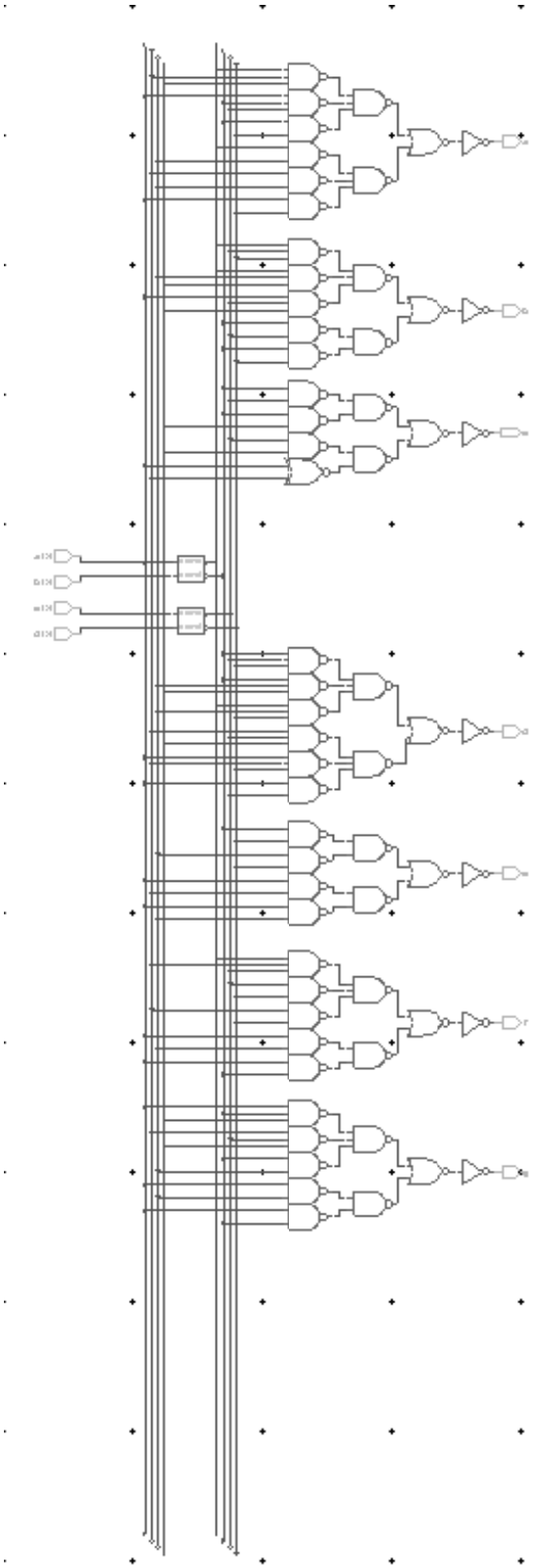
Add/Sub


sel
A_1
B_1
Out_1
A_2
B_2
Out_2
A_3
B_3
Out_3
A_4
B_4
Out_4
A_5
B_5
Out_5
A_6
B_6
Out_6
A_7
B_7
Out_7
A_8
B_8
Out_8
A_9
B_9
Out_9
A_10
B_10
Out_10
A_11
B_11
Out_11
A_12
B_12
Out_12
A_13
B_13
Out_13
A_14
B_14
Out_14
A_15
B_15
Out_15
A_16
B_16
Out_16
Carry_out

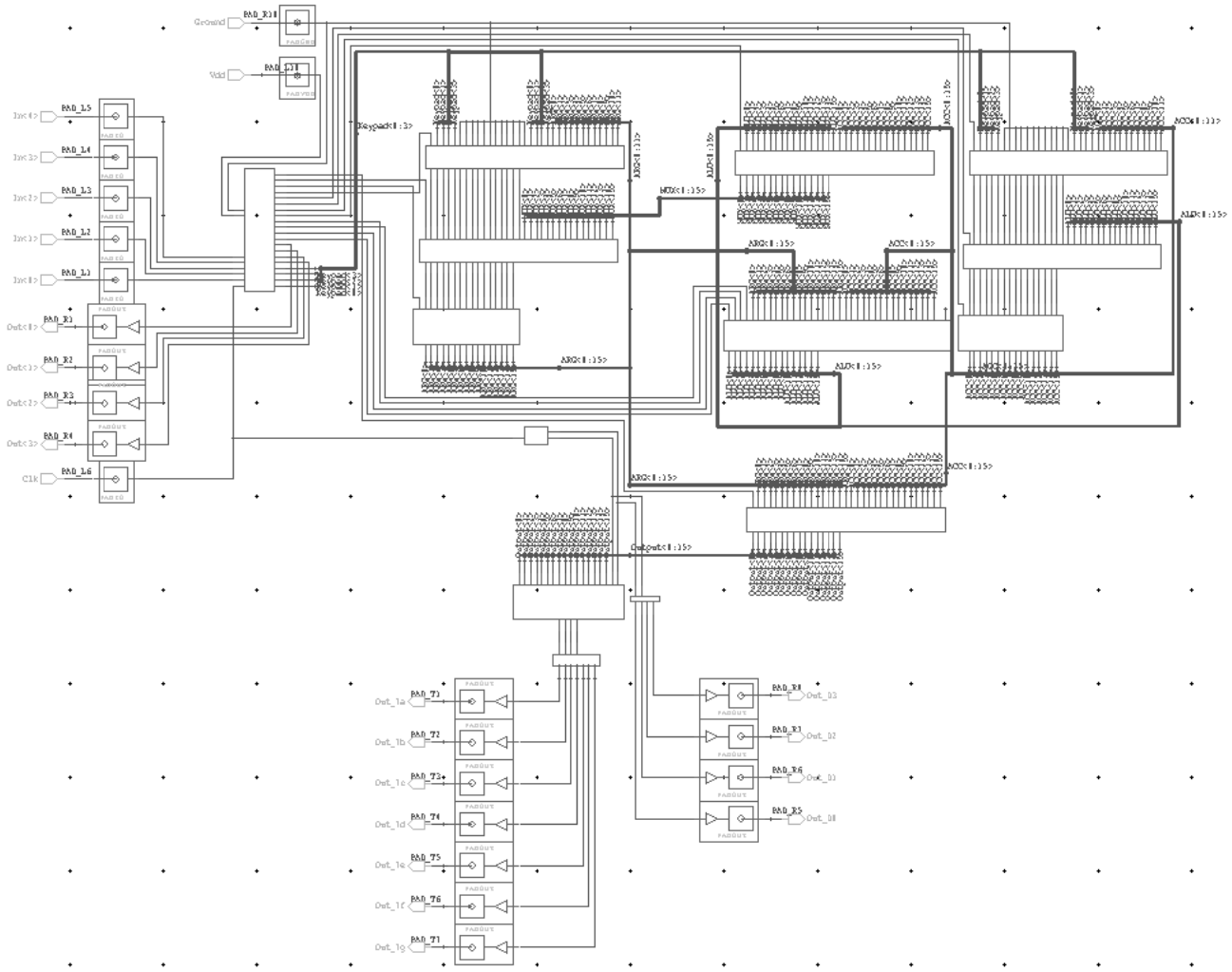
Multiplier



Output Decoder/Display



System Integration



IX. System Integration Layout