Brown University
Division of Engineering
EN1600 Design and Implementation of VLSI Systems. Spring 2008.
Prof. Sherief Reda
Assignment #3.
Due Date: Friday, February 22nd. Points [60 points]

1. [10 points] Generate the I-V characteristics of the following configurations (at temp=70 C):
   a. [1 point] A W=4λ, L=2λ NMOS transistor using TSMC 180nm, and AMI 0.5micron process technology SPICE models. Remember to adjust your supply voltage according to the process (3.3V @ 0.5micron and 1.8V @ 180nm).
   b. [2 points] Calculate the threshold voltages for the different process technologies.
   c. [1 points] Repeat (a) but instead use W=4λ, L=2λ PMOS transistor. How do you compare the PMOS currents to the NMOS currents at the same input voltages?
   d. [2 points] Repeat (a) using W=6λ and 8 λ (just use 0.5 micron models). What is the impact of width on the current?
   e. [2 points] Repeat (a) using L=4 λ, 6 λ, 8 λ (just use 0.5 micron models). What is the impact of increasing the length of the transistor?
   f. [2 points] Repeat (a) with body biases (+0.2, +0.1V and -0.1V, -0.2V) using 0.5 micron models. What is the impact of the body bias on the threshold voltage and saturation current?

2. [20 points] To model the operation of the transistor, we have considered in class two models: the Shockley model and the alpha-law model. The objective of this exercise is to test the accuracy of these two models in comparison to SPICE results. This question ultimately seeks to produce similar plots as in Figure 2.17 of your textbook or as in Slide 6 of lecture 8. For this problem, assume VDD=3.3V, electron mobility (U0) is 447 cm2/V, oxide thickness (tox) 14.1 nm, temperature = 27 C, W = 1 micron, and L = 0.5 micron. SiO2 permittivity is 3.4 times that of free space.

   a. [4 points] Write down the Shockley model and the alpha-law model. Explain the shortcomings of the Shockley model and describe the main motivations behind the alpha model.
   b. [2 points] Use SPICE to plot the IV characteristics of an NMOS transistor of W = 1 micron and L = 0.5 micron using the SPICE models of the AMI 0.5 micron process. Plot the results using a sweep from Vgs = 0V to Vgs = 3.3V in steps of 0.3V.
   c. [6 points] Use the Shockley model to predict and plot the IV characteristics of the the same NMOS transistor of part (b) at Vgs = 3.3V and Vgs = 2.4V. You might like to use a tool like MATLAB to automate the plot generation process. To compare the results of the Shockley model versus the SPICE results, it would be ideal if you can superimpose your Shockley model plots on the plots form part (b) (similar to Figure 2.17). Comment on the accuracy of the Shockley model.

d. [8 points] To use the alpha model, you need to empirically determine its various parameters (e.g., alpha, Pc, ..., etc). Use the SPICE results from part (b) to estimate the various parameters of the alpha model. Plot the alpha-model IV results at Vgs = 3.3V and Vgs = 2.4V, and compare its predictions against the Shockley model. It would be ideal if you impose your plots on the ones from parts (b) and (c).

2. [30 points] Compact layout of complex gates is important for total area minimization. Assuming horizontal power (VDD and GND) lines, and vertical polysilicon lines for the inputs:

a. [6 points] Draw the stick diagram of the gate $x = \overline{(a+b)\cdot c}$ using the following two different polysilicon input orderings: (a c b) and (a b c).
b. [2 points]. How many uninterrupted active diffusion strips are required for each ordering?
c. [2 points]. Which input ordering uses less gate area?
d. [4 points]. Construct the layout that gives the minimum area using Tanner L-Edit. Report the layout, dimensions and the DRC results.
e. [4 points]. Extract the circuit layout to SPICE and verify the functionality of the circuit by simulating all possible input combinations in SPICE and report the input and output waveforms.

The answers to the previous subquestions demonstrate that input ordering impacts the number of uninterrupted diffusion strips and consequently the area of the gate. It is always best to find the optimal input ordering that leads to the minimum gate area. To achieve this goal, we will use some techniques from graph theory. A graph is a set of nodes and a set of edges. The edges connect the nodes; i.e., each edge connects two nodes. To find the optimal input ordering, construct a graph where the vertices represent the nodes (or signals) of the circuit given by x and the edges represent the transistors.

d. [4 points] Draw the pull-up graph and the pull-down graph for x separately.
e. [4 points] A path in a graph is a sequence of edges such that no edge is repeated. What is the characteristic of the path(s) that leads to the optimal ordering of inputs?
f. [4 points] Without drawing the stick diagram of the function, find the optimal input ordering that minimizes the area of gate y $y = \overline{ab + cd}$.