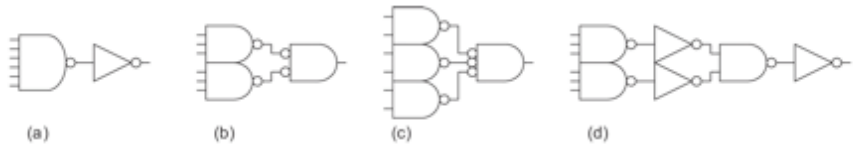
Brown University
Division of Engineering
EN1600 Design and Implementation of VLSI Systems. Spring 2008.
Prof. Sherief Reda
Assignment #4. Due Date March 7th
Total 60 points

1. [5 points] Calculate the logical effort of a 2-input XOR gate.

2. [5 points] In the lecture we proved that for a path of two stages, the least path delay is achieved when the effort of the two stages is equal. Generate this proof to show that the least delay in a path of *N* stages results when all stages bear the same effort.

3. [5 points] Consider four designs of a 6-input AND gate in the next figure. Develop an expression for the delay of each path if the path electrical effort is H. What design is fastest for H=1? For H=5? For H=20? Explain your conclusions.



4. [5 points] A 180 nm standard cell process can have an average switching capacitance of 150 pF/mm^2. You are synthesizing a chip composed of random logic with an average activity factor of 0.1. Estimate the power consumption of your chip if it has an area of 70 mm^2 and runs at 450 MHz at V_{dd} = 0.9V.

5. [5 points]. Consider a 5 mm long, 4 λ-wide metal2 wire in 0.6µm process. The sheet resistance is 0.08 Ω/▪ and the capacitance is 0.2 fF/µm.

a. [2 points] Construct a 3-segment π-model for the wire.
b. [3 points] A 10× unit-size inverter drives a 2× inverter at the end of the 5 mm wire. The gate capacitance is C = 2 fF/µm and the effective resistance is R = 2.5 kΩ.µm for nMOS transistors. Estimate the propagation delay using Elmore delay model; neglect diffusion capacitance.

6. [30 points] The design of any circuit starts first with the **design and characterization** of a standard cell library at AMI 0.5µ technology. In this exercise you will collaborate on implementing a standard cell library. To make all cells interoperable, i.e., can be abutted horizontally, all cells must be exactly of height 53λ. For your assignment, your must report the following:

a. [4 points] Draw the transistor schematic for your cell, and label each transistor with its size.
b. [5 points] Using L-Edit, implement the **layout** of your cell together with the **dimensions** and its **area**. Include the **DRC** report.

c. [5 points] **Extract** the circuit layout into **SPICE** and **verify** its functionality and build its truth table. Make sure to check the inclusion of parasitics when you extract to SPICE.
d. [6 points] Use SPICE to **characterize** the cell **timing** characteristics as a function of the load. For each transition 0→1 and 1→0, draw a curve that gives the propagation delay as a function of the load capacitance. Then using linear fitting to the curve, derive an empirical formula that calculate the delay as a function of the load capacitance. Relate your equation to the logical effort model we studied in class.
e. [6 points] Use SPICE to calculate the gate **input capacitance** per pin. You might like to read more of Subsection 5.4.3 of your book to get an idea of how to achieve this in SPICE.
f. [4 points] Using SPICE, characterize the cell **energy** consumption per transition.

➡ We will divide the collaboration for the library as follows.

- Aaron: AO22 (And-Or Gate)
- Aung: BUFF (buffer)
- Caitlin: BUFZ (tri-state buffer)
- Chaka: DFF (D Flipflop)
- Holiano: INV (1x size) and MUX (a 2 by 1 multiplexor)
- Phong: NAND2 and NAND3
- Ro-To: NOR2 and NOR3
- Ryan: XOR2 (XOR gate with two inputs)