

Brown University  
Division of Engineering  
EN1600 Design and Implementation of VLSI Systems. Spring 2008.  
Prof. Sherief Reda  
Assignment #5. Anytime before Spring break.  
Total 10 points

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Note: Please use questions 1 - 6 as self-paced exercises as the solutions are provided. Question 7 is related to the previous assignment and it is worth 10 points.

1. The path from the data cache to the register file of a microprocessor involves 500ps of gate delay and 500ps of wire delay along a repeated wire. The chip is scaled using constant field scaling and reduced height wires to a new generation with  $S = 2$ . Estimate the gate and wire delays of the path. By how much did the overall delay improve?
2. Using the data sheet from Figure 4.25 of your textbook, find the rising and falling logical effort and parasitic delay of the X1 2-input NAND gate from the A input.
3. Design an asymmetric 3-input NOR gate that favors a critical input over the other two. Choose transistor sizes so the logical effort on the circuit input is 1.5. What is the logical effort of the noncritical inputs?
4. Sketch a pseudo-nMOS gate that implements the complement of the function  $A(B+C+D)+E \cdot F \cdot G$
5. Sketch a 3-input dual-rail domino OR/NOR gate.
6. Redesign the memory decoder from Section 4.3.4 using footed domino logic. You can assume you have both true and complementary monotonic inputs available, each capable of driving 10 unit transistors. Label gate sizes and estimate delay.
7. [10 points] Compare and contrast your standard cell design with the one provided in the Tanner library. Compare the following items:
  1. The layout and dimensions of the cells and transistors.
  2. The delay and timing characterization.
  3. The input pin capacitance.