1. [15 pts] Consider the path in the following figure using flip-flops F1, F2, and F3. The flip-flops have a setup time of 0.1ns and a clock-to-Q delay of 0.15ns. There is no skew between the clocks $\Phi_{1a}$, $\Phi_{1b}$, $\Phi_{1c}$ that all share the same start time. The departure time from each flop is $D_1=D_2=D_3=0$.

   a. [5 pts] What is the minimum cycle time at which the system operates correctly?
   b. [10 pts] Suppose that $\Phi_{1a}$ and $\Phi_{1b}$ are in a common local clock domain, but $\Phi_{1c}$ is in a different clock domain. What is the minimum cycle time of the system if
      i. [5 pts] The local skew is 50ps and the global skew is 140ps?
      ii. [5 pts] The local skew is 25ps and the global skew is 300ps?

2. [25 pts] This exercise asks you to design a prototype for a 4 bit Full Adder (FA) IC. Here are the steps you need to follow and report on.

   a. [5 points] Using the 0.5 micron AMI standard cell library, design a 1-bit FA adder using S-Edit. Create a symbol out of your 1-bit FA. Include a snap shot of your design.
   b. [5 points] Using the 1-bit FA you designed, create a 4-bit FA using S-Edit. Include a snap shot of your design
   c. [5 points] Export your S-Edit design to Tanner L-Edit and complete all layout and routing steps. Report the total number of wire length used as well as the dimensions of your layout. Include a snapshot of your design.
   d. [5 points] Export your layout to SPICE (make sure to extract the parasitics), and verify the functionality of your design by simulating a few random input vectors and making sure that the output patterns of the adder are calculated correctly.
   e. [5 points] Calculate the worst case propagation delay of your adder. Note that different input patterns will lead to different propagation delays. What is the input vector that leads to the worse delay? You do not need to try all combinations to figure out the pattern that exercise the worst case delay!