Brown University
Division of Engineering
EN1600 Design and Implementation of VLSI Systems. Spring 2008.
Prof. Sherief Reda
Assignment #7 (Total 40 points).
Questions 1, 2, and 3 are due on Friday April 25th.
Question 4 is due on Monday April 28th.

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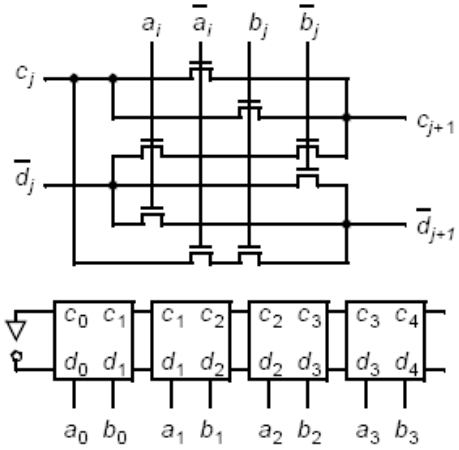
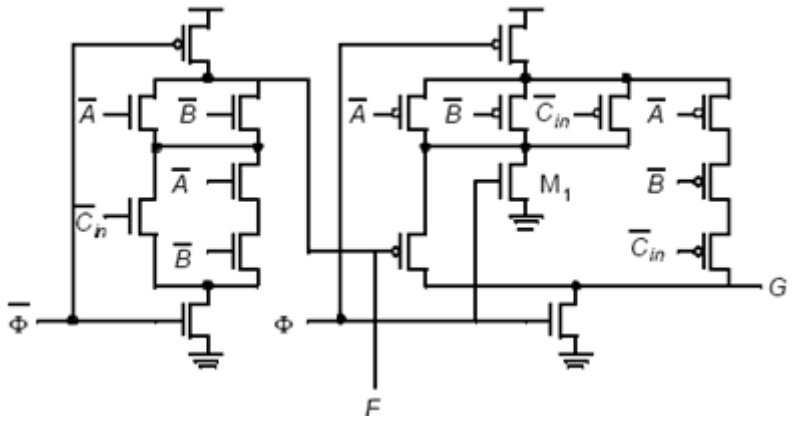
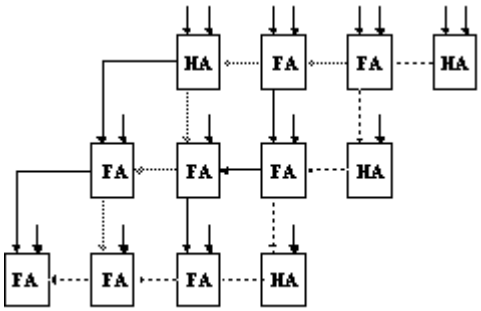
1. [10 pts] Show how the arithmetic module in the following figure can be used as a comparator. Derive an expression for its propagation delay as a function of the number of bits.



2 [10 pts] Consider the dynamic logic circuit in the following figure.
a. [5 pts] What is the purpose of transistor M_1? Is there another way to achieve the same effect, but with reducing capacitive loading on the clock Φ?
b. [5 pts] How can the evaluation phase of F be sped up by rearranging transistors? No transistors should be added, deleted, or resized.



3. [10 pts] An array multiplier consists of rows of adders, each producing partial sums that are subsequently fed to the next adder row as shown in the following figure. In this problem, we consider the effects of pipelining such a multiplier by inserting registers between the adder rows.
a. [3 pts] Redraw the figure by inserting word-level pipeline registers as required to achieve maximal benefit to throughput for the 4x4 multiplier. Hint: you must use additional registers to keep the input bits synchronized to the appropriate partial sums.
b. [3 pts] Repeat for a carry-save, as opposed to ripple-carry, architecture.
c. [3 pts] For each of the two multiplier architectures, compare the critical path, throughput, and latency of the pipelined and nonpipelined versions.
d. [1 pt] Which architecture is better suited?



4. [10 pts] This question deals with the appropriate sizing of the different transistors in the 6T SRAM cell.

(a) [5 pts] Assume that a 6T SRAM cell stores a value of '0'. During read operation of the 6T SRAM cell, it is important to ensure *read stability*, by having transistor N1 sized so that it is "stronger" than N2. Express the voltage at node A as a function of the widths of N2 and N1. What is the width ratio that guarantees that A's voltage stays less than 0.4V? Assume 0.25micron technology with Vdd=2.5V and Vth=0.4V.

(b) [5 pts] Assume that the 6T SRAM cell stores a '1'. During a write operation of '0' to the 6T SRAM cell, it is important to ensure *write stability*, by having transistor N2 sized so that it is stronger than P1. Express the voltage at node A as a function of the widths of N2 and P1. What is the width ratio that guarantees that A's voltage becomes less than 0.4V? Assume 0.25micron technology with Vdd=2.5V and Vth=0.4V.