Core Engineering Program: ABET Course Outcomes

Course: EN160 – Design and Implementation of Very Large-Scale Integrated Systems
Instructor: Professor S. Reda
Revision Date: Spring 2007

Course Description: VLSI (Very Large Scale Integration) CMOS (Complementary Metal Oxide Semiconductor) technology is the main driver of our digital revolution. The goal of the course is to learn how to design and implement VLSI digital circuits and optimize them with respect to different objectives such as area, speed, and power dissipation. Design and analysis will be carried out using computer-aided tools.

Prerequisite: EN163, or instructor permission

Outcomes: Students completing EN160 shall:

1. Have the ability to synthesize static and dynamic logic cells based on knowledge of MOS device physics, modeling, and circuit topologies.
   Addresses ABET outcomes (a), (b), (c), (e), (k)
   Assessment: Design project, student survey

2. Be capable of designing and implementing combinational and sequential CMOS digital circuits and optimize them with respect to different constraints, such as area, delay, power, or reliability.
   Addresses ABET outcomes (a), (b), (c), (e), (k)
   Assessment: Design project, student survey

3. Be capable of implementing a complete design verification process using computer-automated tools for layout, extraction, simulation, and timing analysis.
   Addresses ABET outcomes (a), (b), (c), (e), (k)
   Assessment: Design project, student survey

4. Design and verify a prototype silicon integrated circuit suitable for fabrication using the AMI 0.8- μm CMOS process.
   Addresses ABET outcomes (a), (b), (c), (e), (k)
   Assessment: Design project, student survey

Core Engineering Program – ABET course outcomes student survey

Course: EN160 – Design and Implementation of VLSI Systems

Outcomes: Please rate your understanding of, and ability to apply, the knowledge and skills listed in the outcomes for this course.

	Weak				Proficient
1 – Synthesize Logic Cells	1	2	3	4	5
2 – Constraint Design	1	2	3	4	5
2 – Design Verification	1	2	3	4	5
3 – Prototype IC Design	1	2	3	4	5

Course Evaluation: Please rate the various components of this course in helping you develop and apply the knowledge and skills listed in the course outcomes.

1: Synthesize Logic Cells					
	Not helpful				Very helpful
Lectures	1	2	3	4	5
Project	1	2	3	4	5
Homework	1	2	3	4	5
Laboratories	1	2	3	4	5
Exams	1	2	3	4	5

2. Constraint Design				
Not helpful				Very helpful
1	2	3	4	5
1	2	3	4	5
1	2	3	4	5
1	2	3	4	5
1	2	3	4	5

3: Design Verification					
	Not helpful				Very helpful
Lectures	1	2	3	4	5
Project	1	2	3	4	5
Homework	1	2	3	4	5
Laboratories	1	2	3	4	5
Exams	1	2	3	4	5

4: Prototype IC Design				
Not helpful				Very helpful
1	2	3	4	5
1	2	3	4	5
1	2	3	4	5
1	2	3	4	5
1	2	3	4	5

Additional Comments: Please use the reverse of this sheet to provide more detailed feedback regarding course outcomes.