Brown University
Division of Engineering
EN0160 Design and Implementation of VLSI Systems. Spring 2007.
Prof. Sherief Reda
Assignment #2. Due Friday Feb 16 2007.

Grading policy: Each item is worth 2 points. A completely wrong/missing answer credit is 0/2; a partial answer is 1/2.

- Please solve 2.2, 2.8, 2.11, 2.12, 2.16, 2.22.

Using smartSPICE, please solve the following.

1. Generate the I-V characteristics of the following configurations (at temp=70):
   a) A W=4λ, L=2λ NMOS transistor using 130nm, 180nm, and AMI 0.5micron process technology SPICE models. Remember to adjust your supply voltage according to the process (5V @ 0.5micron, 1.8V @ 180nm and 1.2V @ 130nm).
   b) In exp (a), what are the "rough" values of threshold voltages for different process technologies? How do you find the saturation currents when the V_{gs} is equal to the supply voltage? Can you generate a plot where x-axis is technology process and y-axis is the saturation current when V_{gs} is equal to supply voltage?
   c) Repeat (a) but instead use W=4λ, L=2λ PMOS transistor. How do you compare the PMOS currents to the NMOS currents at the same input voltages?
   d) Repeat experiment (a) using W=6λ and 8 λ. What is the impact of width on the current? (just use 180nm models).
   e) Repeat experiment (a) using L=4 λ, 6 λ, 8 λ. (just use 180nm models).
   f) Repeat experiment (a) using different temperatures (25 and 125). What is the impact on current? (just use 180nm models).
   g) Repeat experiment (a) with body biases (+0.2, +0.1V and -0.1V, -0.2V). What is the impact of the body bias on the threshold voltage and saturation current? (just use 180nm models).

2. Generate voltage transfer characteristics of an inverter with PMOS W=8 λ and L=2 λ and NMOS W=4 λ and L=2 λ. Calculate the low and high noise margins. Try PMOS width W=4 λ and W=12 λ and recalculate the noise margins. What do you observe? Just use 180nm models.

3. Take the inverter SPICE design and flip the Vdd and Gnd connections. That is, NMOS connected to VDD and PMOS connected to Gnd. What is the logic function of the gate? Generate the voltage transfer characteristic. What is the output voltage when the input voltage is High? Low? Just use 180nm models.

4. **Bonus.** Plot the NMOS transistor gate capacitance as a function of the gate-source voltage. Use 180nm library with temp=70.