Brown University
Division of Engineering
EN0160 Design and Implementation of VLSI Systems. Spring 2007.
Prof. Sherief Reda
Assignment #3 (Total 25 points). Due Friday March 2nd 2007.

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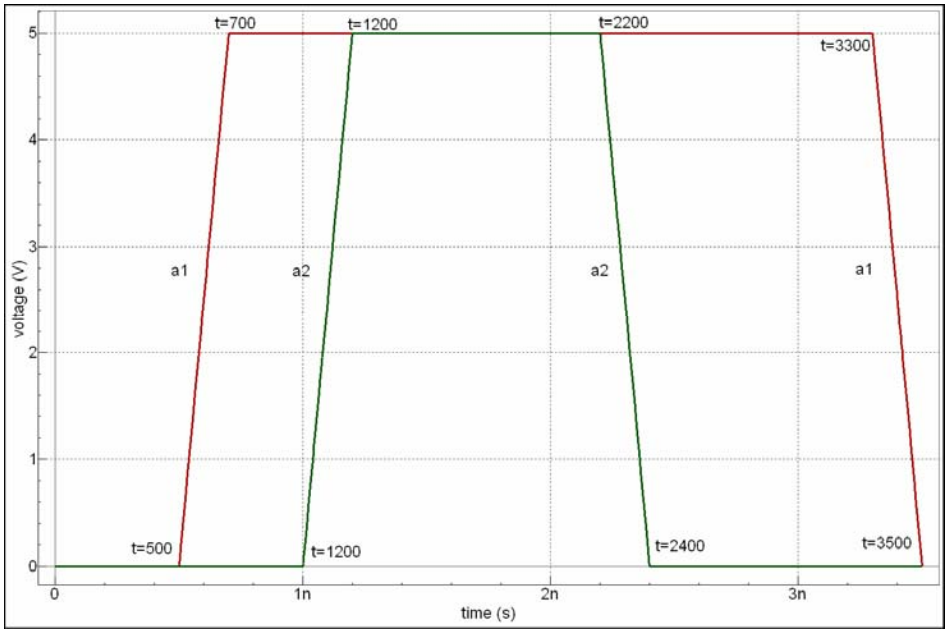
Each question from your textbook is worth 2 points.

- Please solve the following problems: 4.4, 4.10, 4.12, 4.24, 4.28 and 4.32.

In addition, please solve the following three problems using the 0.5micron AMI SPICE models.

1. [Total 7 points] Using SPICE, design a NAND gate with the following parameters (expressed in λ) W=8 L=2 AS='8*5' PS='2*8+10' AD='8*5' PD='2*8+10' for both NMOS and PMOS transistors. The two inputs are labeled a1 and a2. a1 and a2 have the following waveforms



   a) [1 point] Simulate the transient response of your system from 0ps to 3500ps and plot the output waveform. Report the dynamic power (see Subsection 5.5.4).
   b) [2 points] Use SPICE to compute the rise and fall propagation delay in the two cases given in the following table. Explain why there exists delay despite that we did not connect the output of the gate to any load? Explain why the rise delay differs in the two cases? Why is one larger than the other? Explain also the fall case.

	Rise delay	Fall delay
a2 close to the output		
a2 far from the output		

c) [2 points] Connect the output of the NAND gate to a load capacitance and vary the capacitance from 0fF to 50fF in steps of 10fF. Plot the rise delay as function of the load capacitance. What is the function that calculates the rise delay given the load capacitance? (use the case where a2 is far from the output).

d) [2 points] Disconnect the load capacitance (or keep it with 0fF value). Vary a2 fall transition time from 200ps to 600ps in steps of 100ps (e.g., a2 falls from 2200 to 2400, 2500, 2600, 2700, and 2800), and calculate the propagation delay. Does the propagation delay change? Plot the propagation delay as a function of the input transition time. How does this compare to what we took in class? (use the case where a2 is far from the output).

2. [2 points] Using Tanner L-Edit tool, draw a layout for an inverter with PMOS (W=12 λ and L=2 λ) and NMOS (W=6 λ and L=2 λ). Make sure that your design is as compact as possible while following the design rules specified in Chapter 3 as well as the color diagrams on your textbook cover. Generate a SmartSpice netlist from your layout and simulate the generated netlist for all input combinations.
3. [4 points] Design layout for two-input NAND and two-input NOR gates using Tanner L-EDIT. The transistor sizing should be as follows:

	PMOS W	PMOS L	NMOS W	NMOS L
nand2	12λ	2λ	12λ	2λ
nor2	24λ	2λ	6λ	2λ

Extract the circuit netlist of each of the gates and verify the functionality of the gates using SmartSpice.

Notes:

- Remember to check the tutorial in lecture09 and the one available in the class webpage.
- For easy layout, you might want to set the major grid size as 2 λ and the minor grid size as 1 λ by going to Setup → Design and selecting the GRID tab in the TANNER L-EDIT menu. If you have trouble seeing the grid when you zoom out to fit your design on the window, change the `Suppress major/minor grid if less than: x Pixels' to a smaller number from the same menu.