Brown University
Division of Engineering
EN0160 Design and Implementation of VLSI Systems. Spring 2007.
Prof. Sherief Reda
Assignment #4 (Total 24 points). Due Friday March 16th 2007.

Each question from your textbook is worth 2 points.

- Please solve the following problems: 6.8, 6.12, 6.18, 6.28, 6.36, 6.38 and 6.42.

In addition, please solve the following problem using the 0.5micron AMI process technology models.

1. [Total 10 points]. This exercise asks you to design a prototype for a 1 bit Full Adder (FA) IC. Here are the steps you need to follow and report on.
    a) [1 points] Use the gates (inv/nand/nor) you designed in HW3 (after fixing any problems with them) to **synthesize a library of logic cells**. This is a very easy step and amounts to consolidating all gates as cells in one design library (see "Using Hierarchical Design using L-Edit" tutorial on the class webpage).
    b) [4 points] Use the synthesized cells to design a 1 bit FA prototype IC. Complete all **layout** and **routing** required. Please report the total area and total length of wires used by your design. Report your efforts on how you tried to **constrain** the total system area, delay, and power.
    c) [1 points] **Extract** the layout information from L-Edit into SPICE and prepare it for **simulation** by adding the appropriate SPICE decks.
    d) [4 points] **Verify** the correctness of your prototype implementation by simulating all the possible input vectors (8 vectors). For each pattern, report the **output logic values**, the **delays**, and the **average power** consumed. Remember that you have three inputs and two outputs in a FA.