EN164: Design of Computing Systems
Lecture 12: Processor / Single-Cycle Design 1

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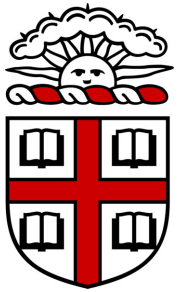
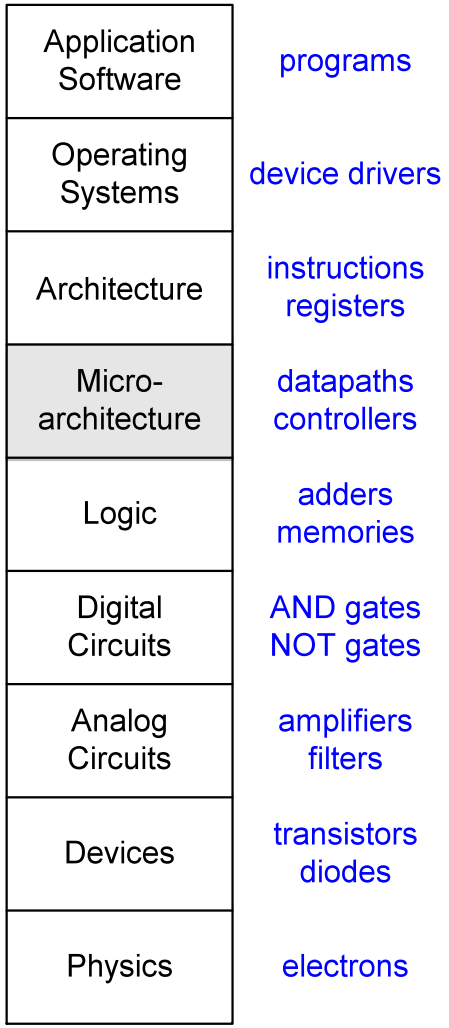


[material from Patterson & Hennessy, 4th ed and Harris 1st ed]

Processor organization (microarchitecture)

- Multiple implementations for a single architecture:
  - Single-cycle
    - Each instruction executes in a single cycle
  - Multi-cycle
    - Each instruction is broken up into a series of shorter steps
  - Pipelined
    - Each instruction is broken up into a series of steps
    - Multiple instructions execute at once.

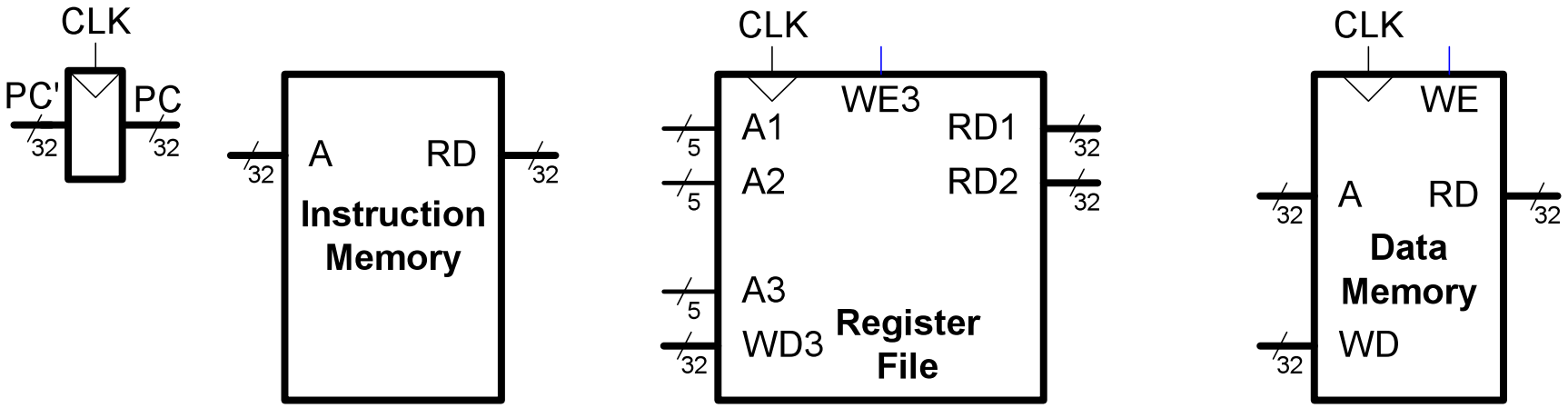


Introduction

- CPU performance factors
  - Instruction count
    - Determined by ISA and compiler
  - CPI and Cycle time
    - Determined by CPU hardware
- We will examine two MIPS implementations
  - A simplified version
  - A more realistic pipelined version
- Simple subset, shows most aspects
  - Memory reference: `lw`, `sw`
  - Arithmetic/logical: `add`, `sub`, `and`, `or`, `slt`
  - Control transfer: `beq`, `j`

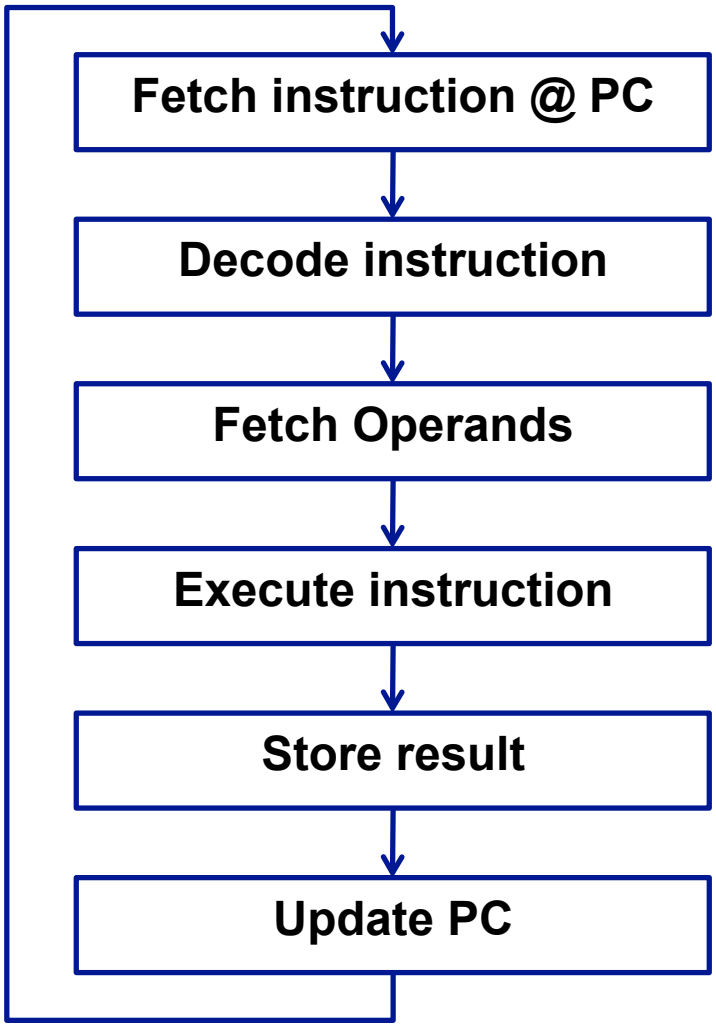
Architectural state

- Determines everything about a processor:
  - PC
  - 32 registers
  - Memory



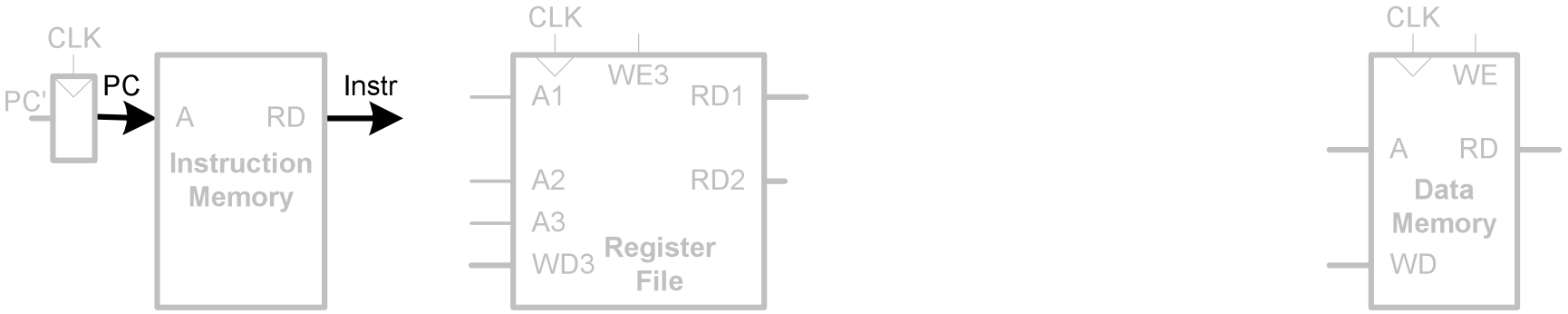
Single-Cycle MIPS Processor

- Datapath
- Control



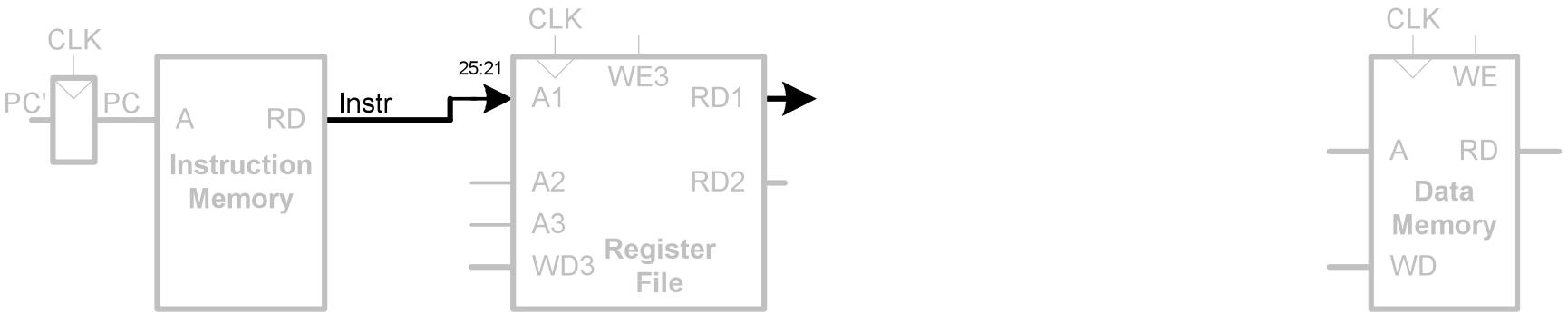
Single-Cycle Datapath: `lw` fetch

- First consider executing `lw`
- **STEP 1:** Fetch instruction



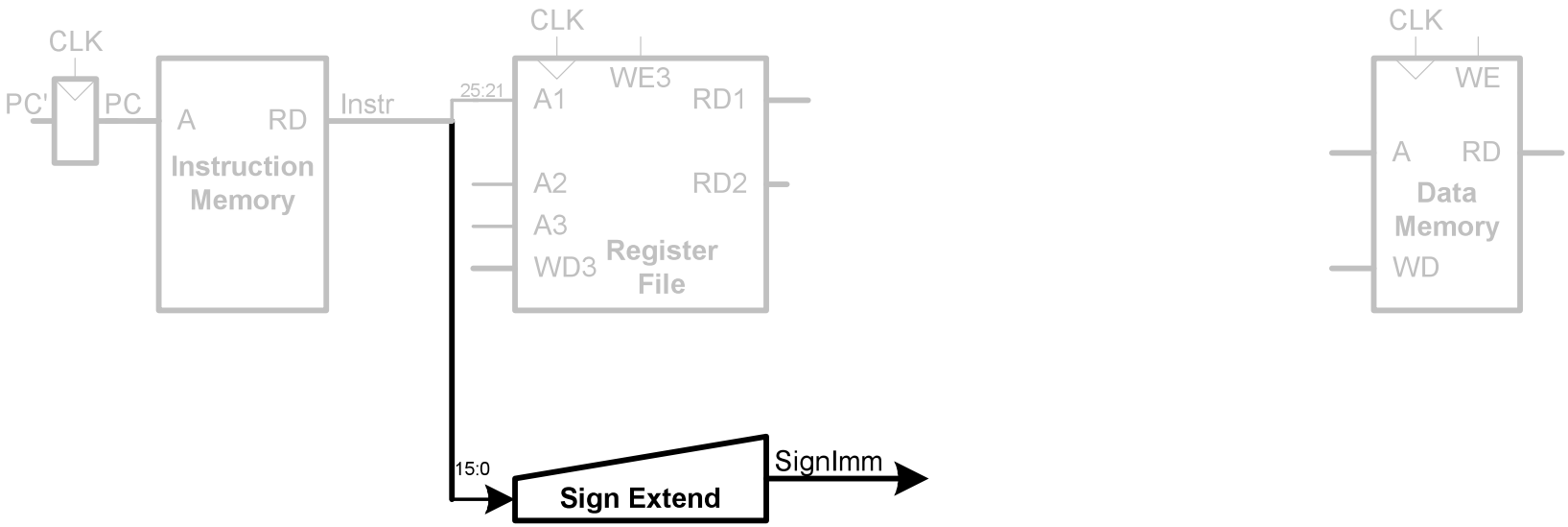
Single-Cycle Datapath: `lw` register read

- **STEP 2:** Read source operands from register file



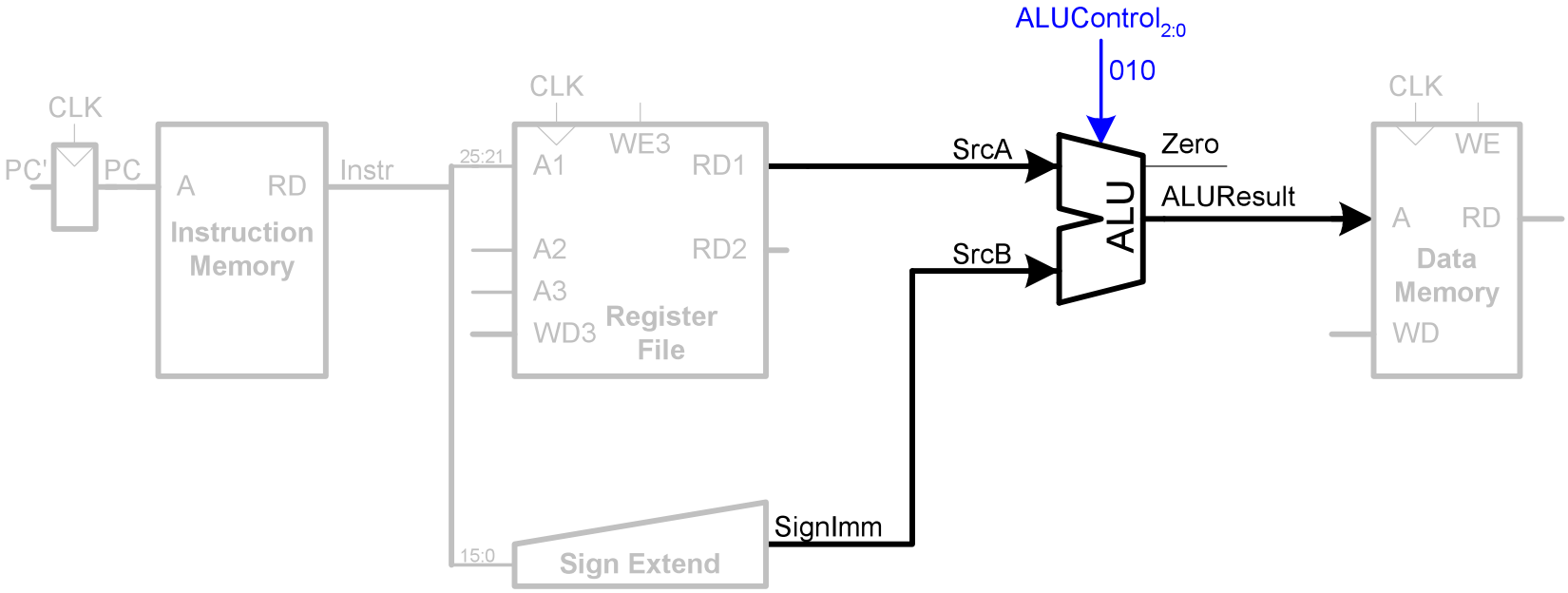
Single-Cycle Datapath: `lw` immediate

- **STEP 3:** Sign-extend the immediate



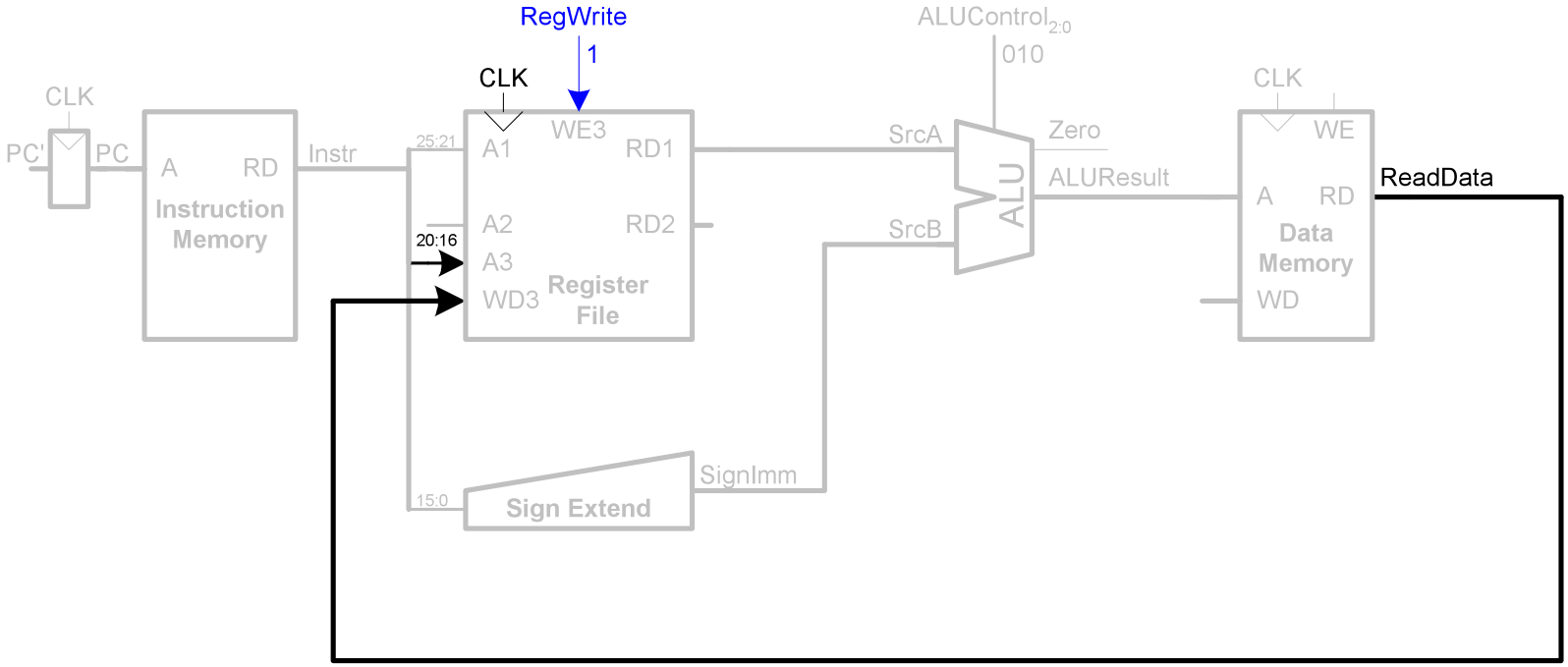
Single-Cycle Datapath: `lw` address

- **STEP 4:** Compute the memory address



Single-Cycle Datapath: `lw` memory read

- **STEP 5:** Read data from memory and write it back to register file



Single-Cycle Datapath: `lw` PC increment

- **STEP 6:** Determine the address of the next instruction