EN164: Design of Computing Systems
Lecture 13: Processor / Single-Cycle Design 2

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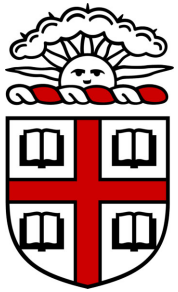
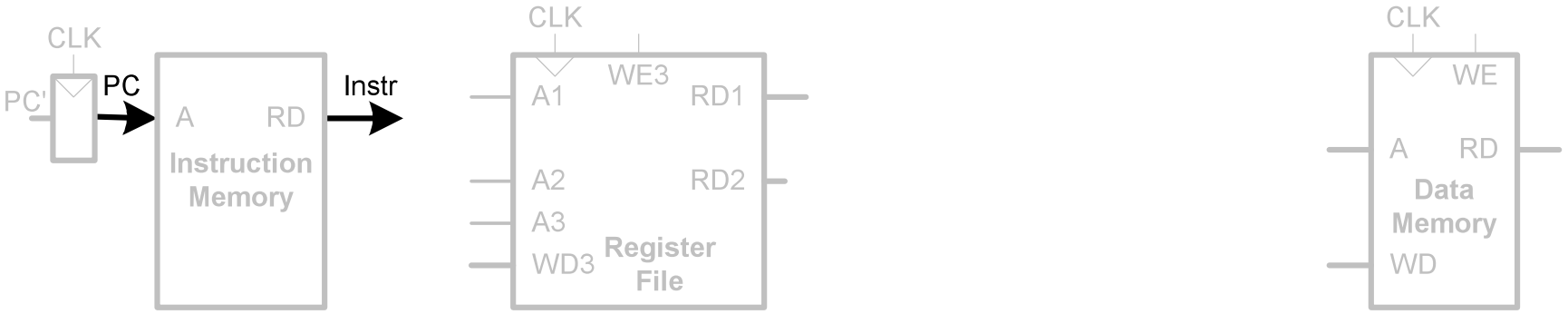


[material from Patterson & Hennessy, 4th ed and Harris 1st ed]

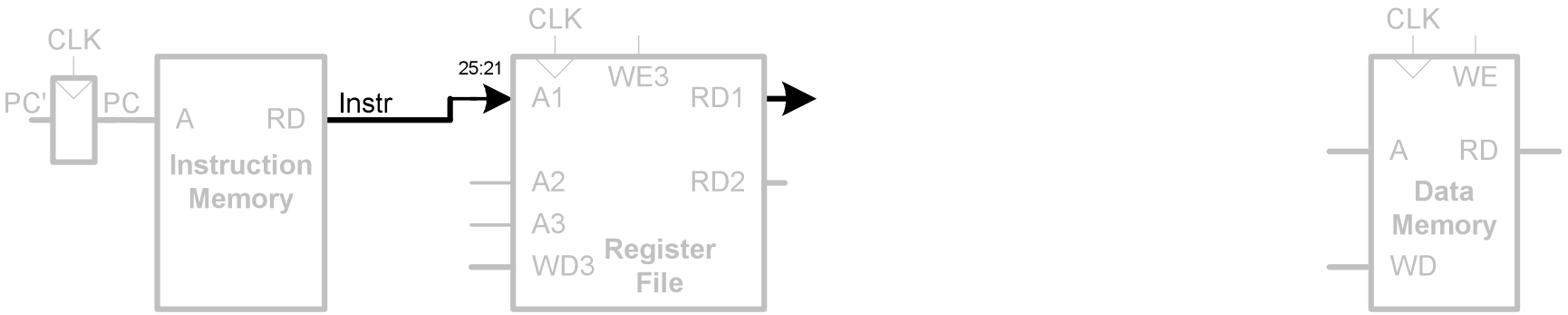
Single-Cycle Datapath: `lw` fetch

- First consider executing `lw`
- **STEP 1:** Fetch instruction



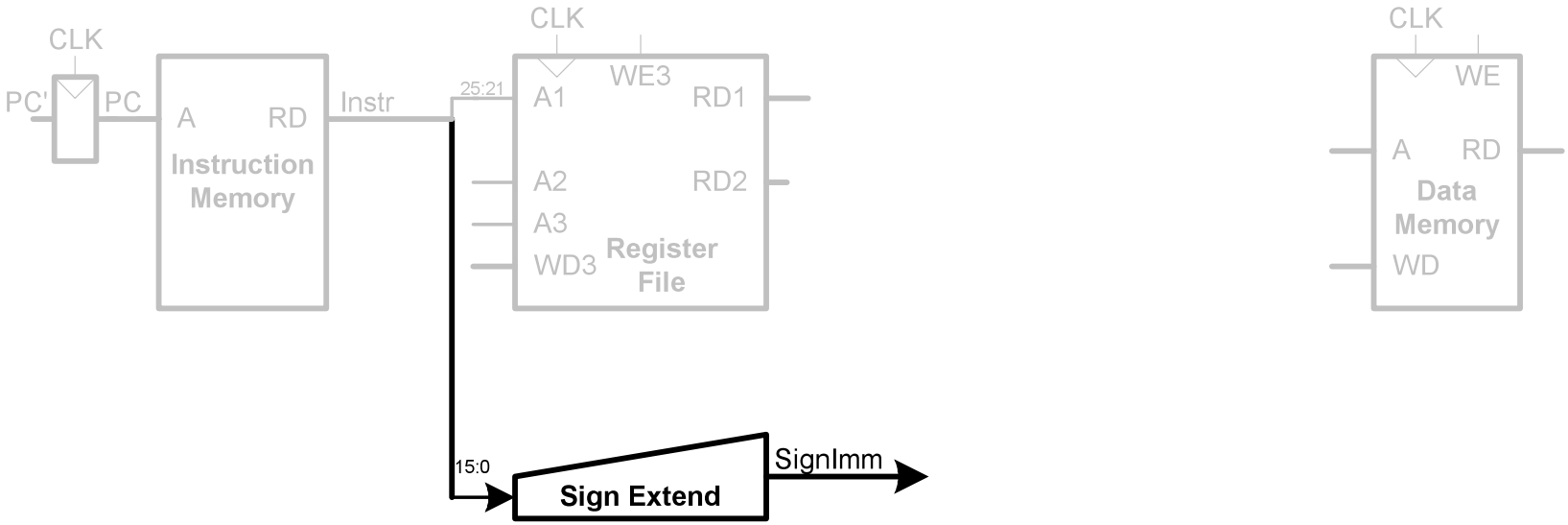
Single-Cycle Datapath: `lw` register read

- **STEP 2:** Read source operands from register file



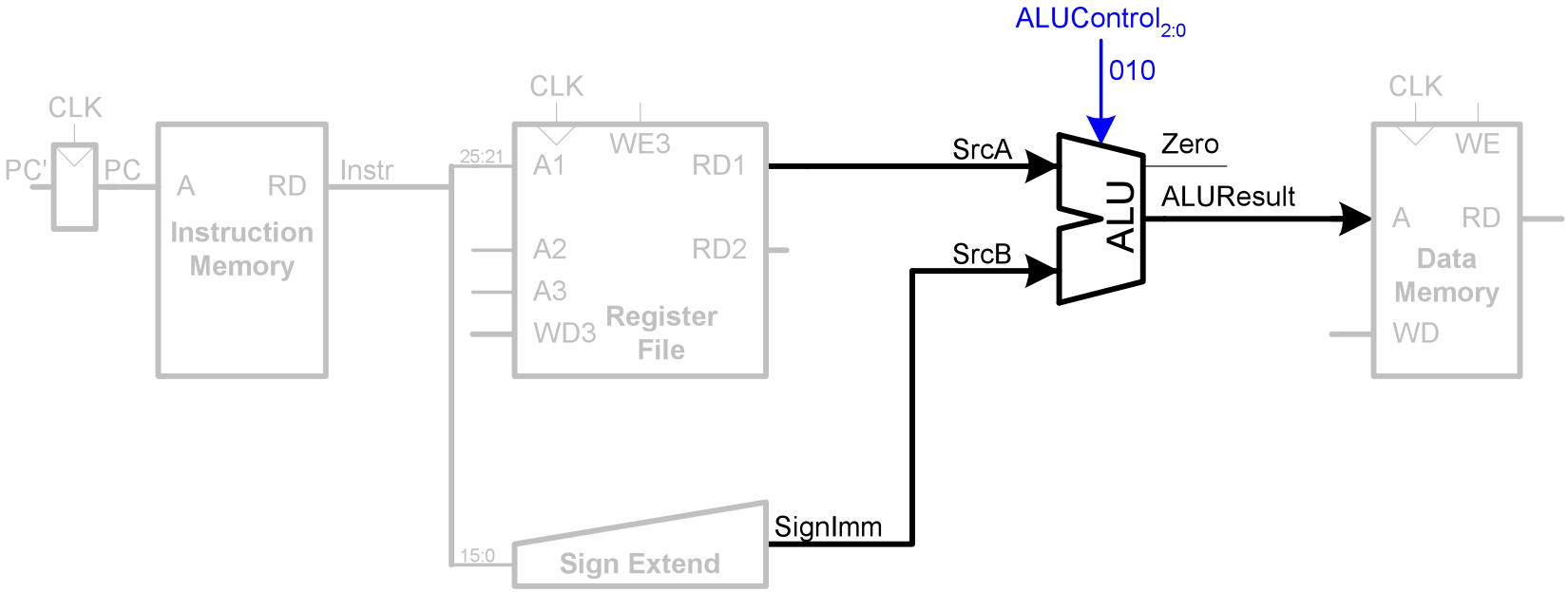
Single-Cycle Datapath: `lw` immediate

- **STEP 3:** Sign-extend the immediate



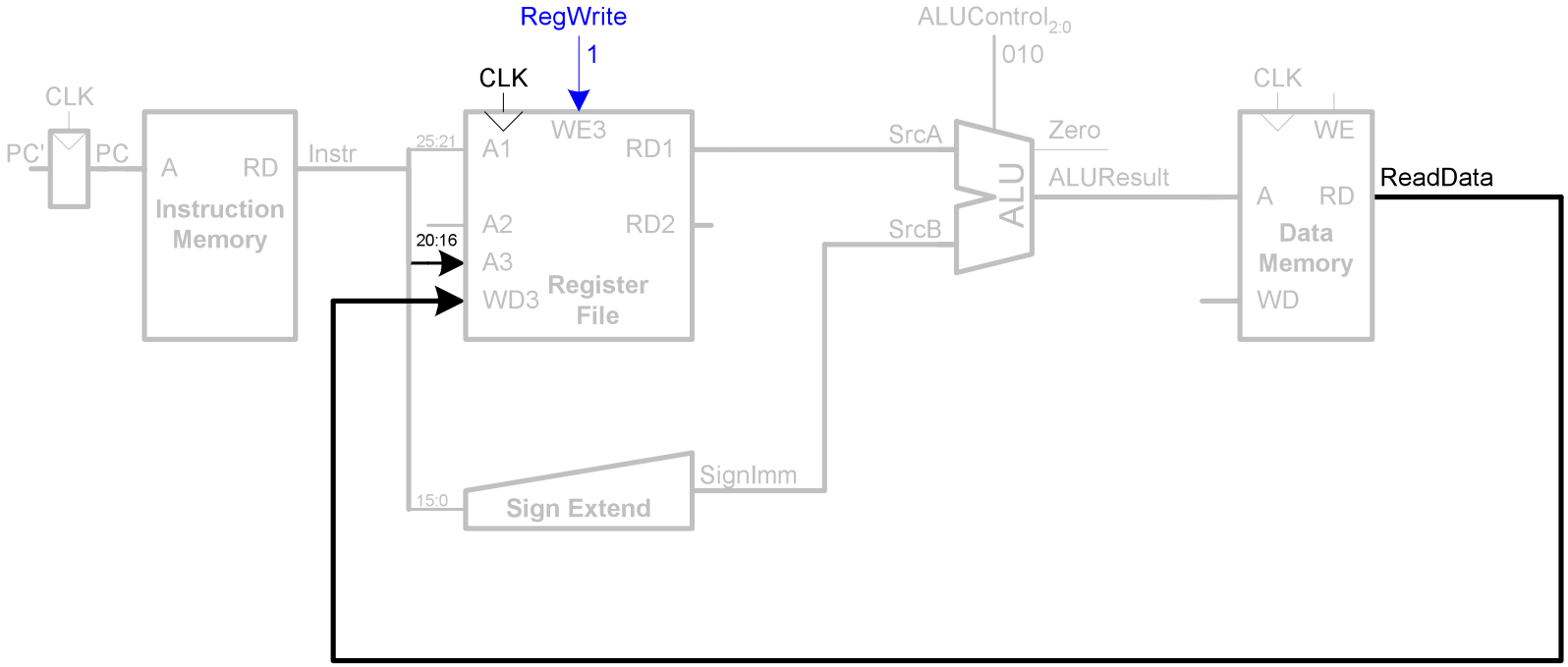
Single-Cycle Datapath: `lw` address

- **STEP 4:** Compute the memory address



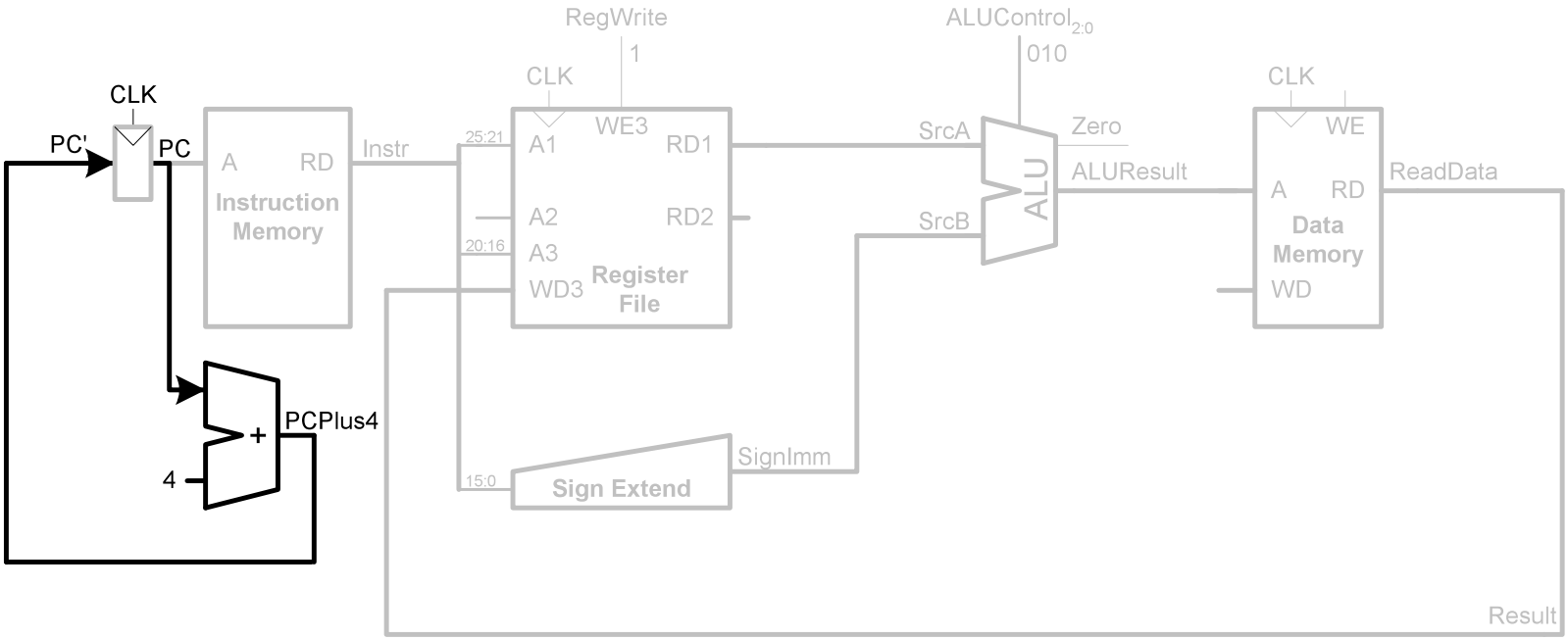
Single-Cycle Datapath: `lw` memory read

- **STEP 5:** Read data from memory and write it back to register file



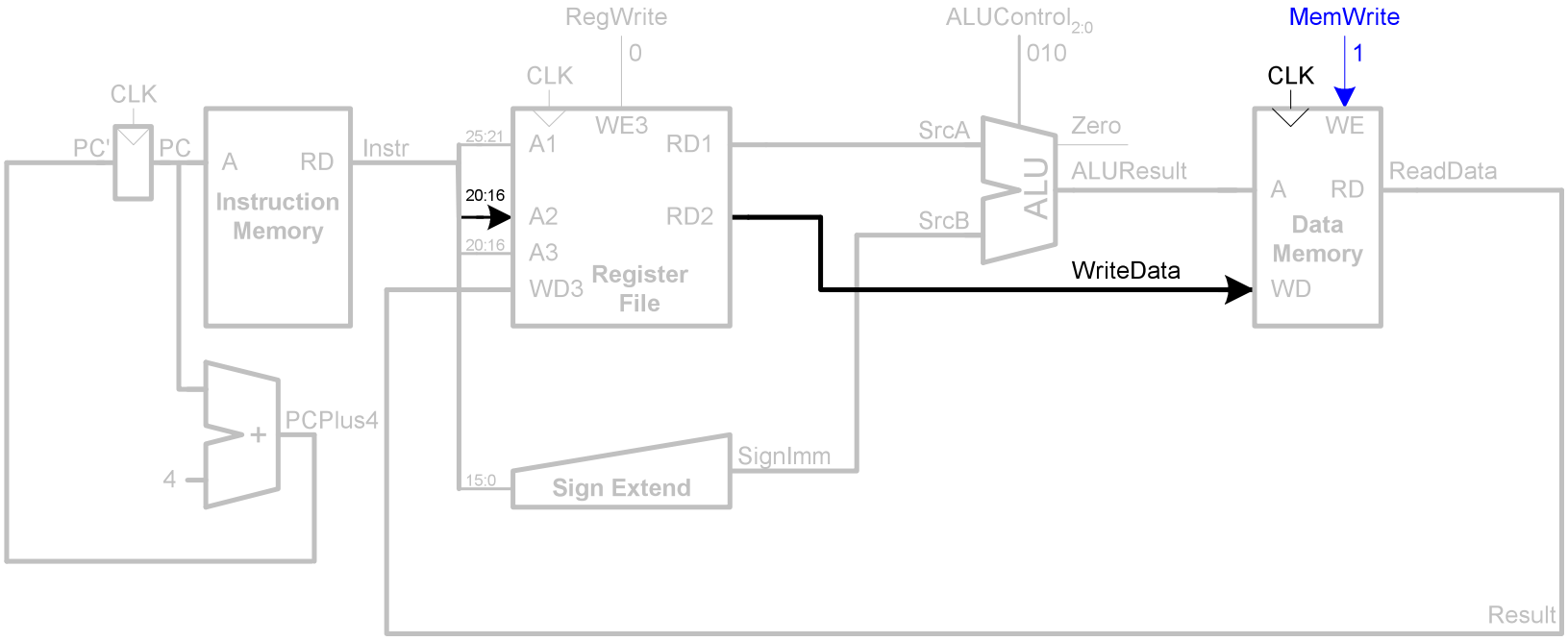
Single-Cycle Datapath: `lw` PC increment

- **STEP 6:** Determine the address of the next instruction



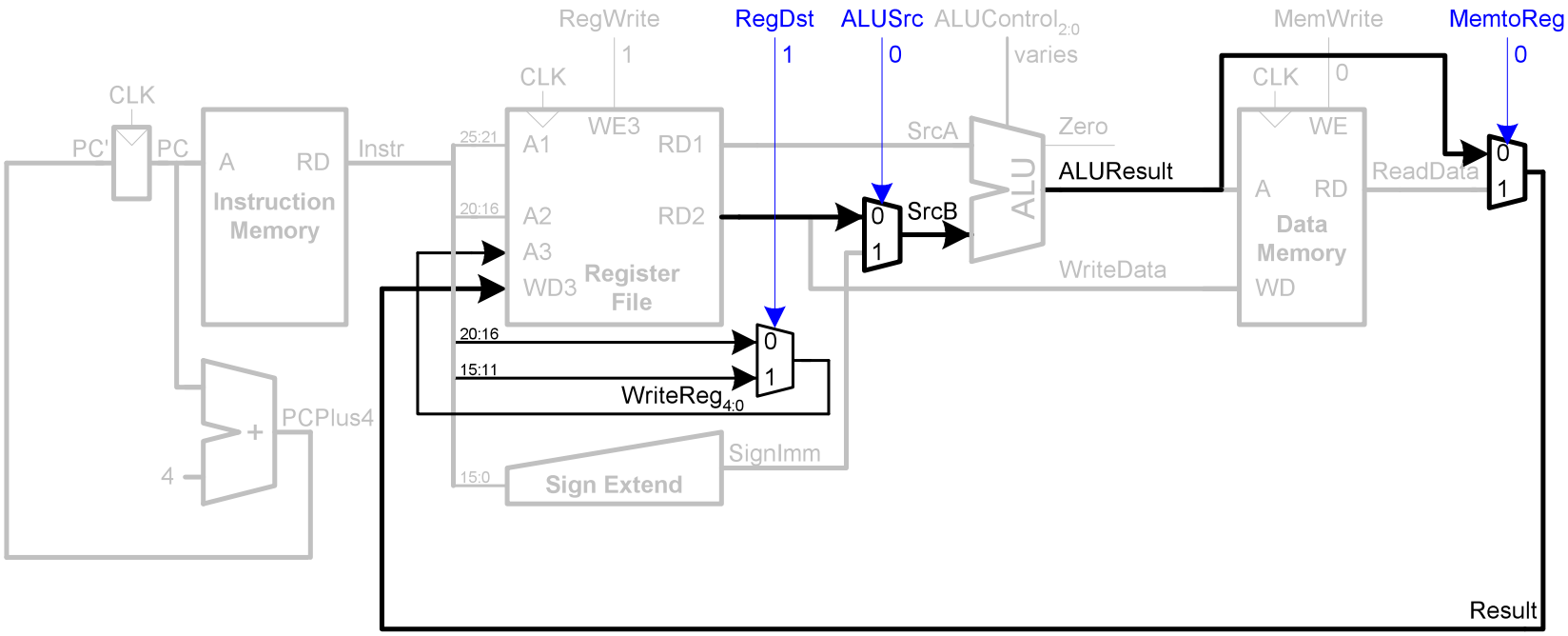
Single-Cycle Datapath: `sw`

- Write data in `rt` to memory



Single-Cycle Datapath: R-type instructions

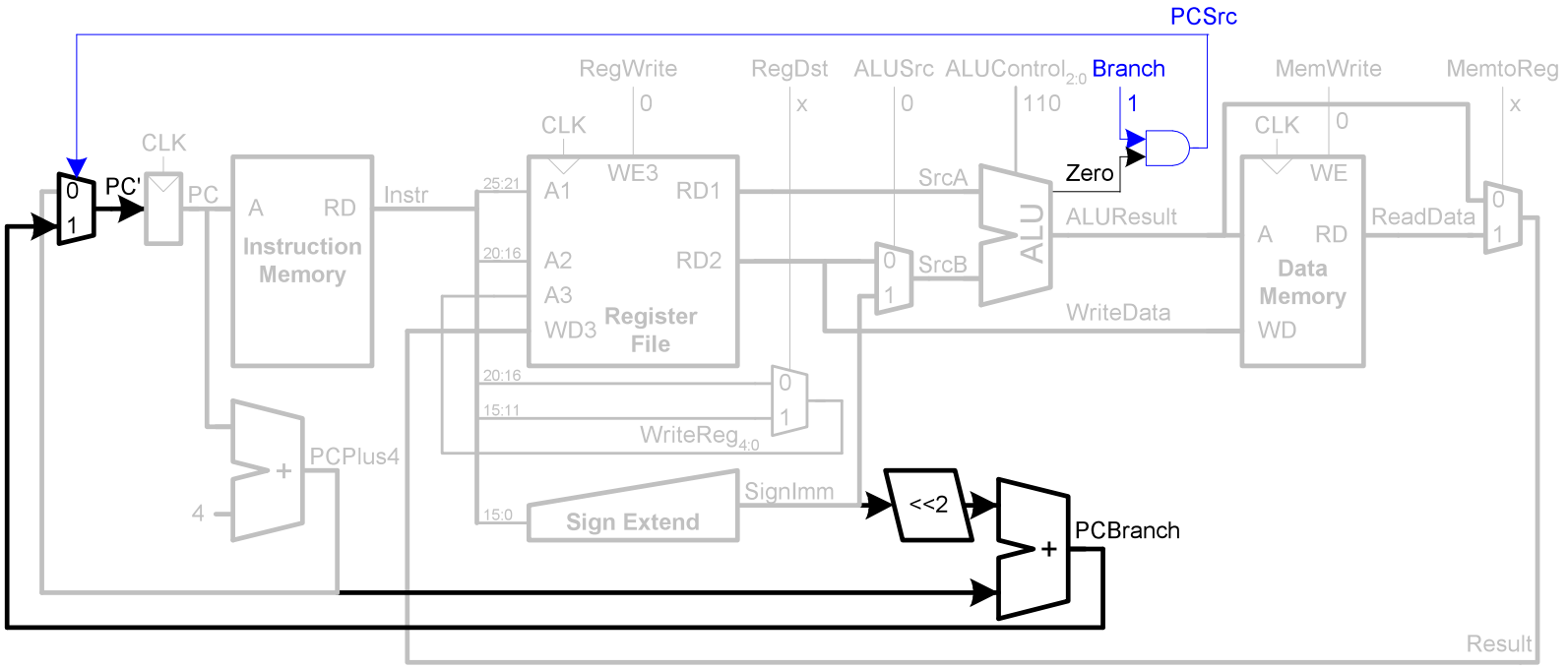
- Read from `rs` and `rt`
- Write *ALUResult* to register file
- Write to `rd` (instead of `rt`)



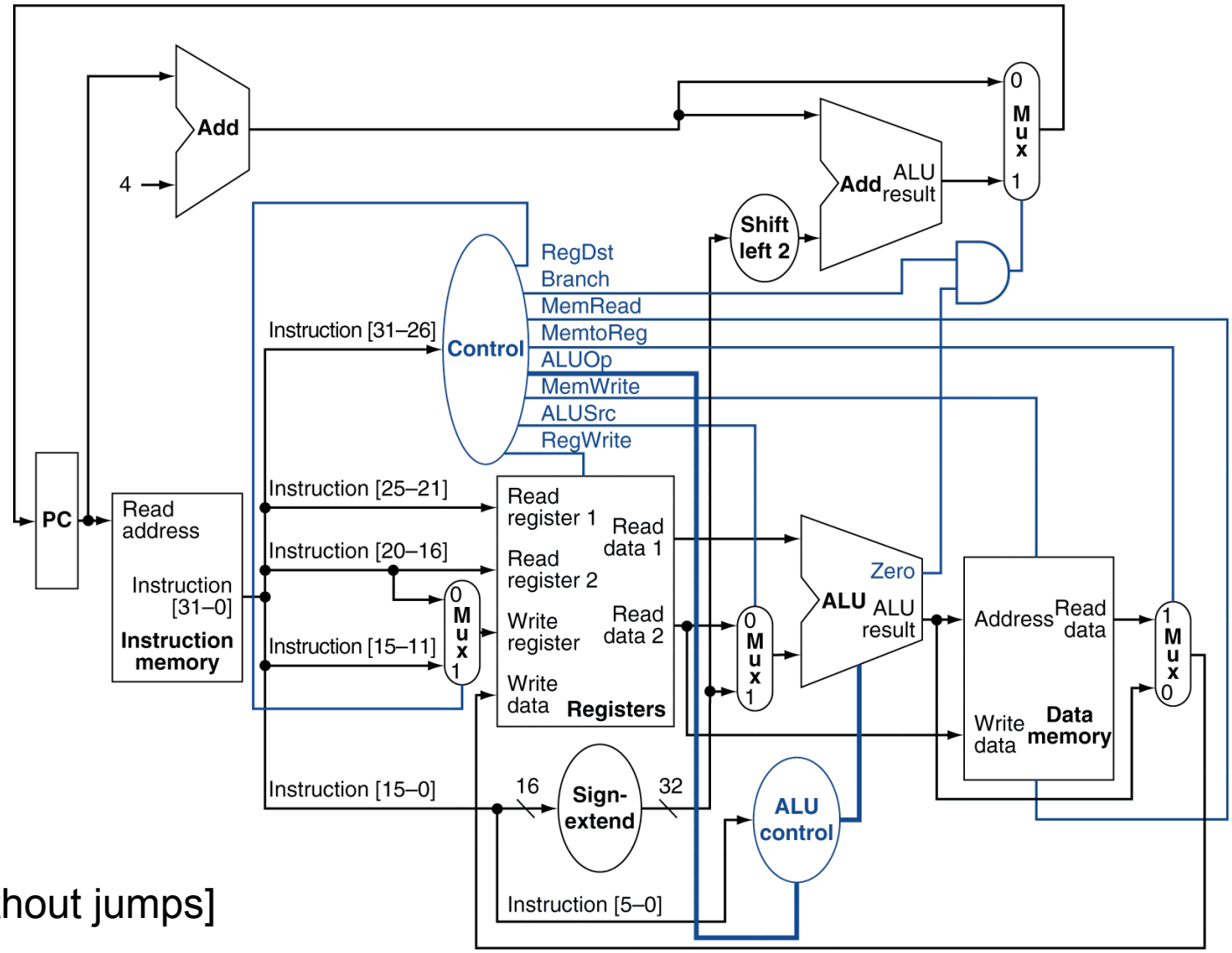
Single-Cycle Datapath: `beq`

- Determine whether values in `rs` and `rt` are equal
- Calculate branch target address:

  BTA = (sign-extended immediate << 2) + (PC+4)



Complete single cycle processor



[without jumps]

ALU control

- ALU used for
  - Load/Store: F = add
  - Branch: F = subtract
  - R-type: F depends on funct field

ALU control	Function
0000	AND
0001	OR
0010	add
0110	subtract
0111	set-on-less-than
1100	NOR

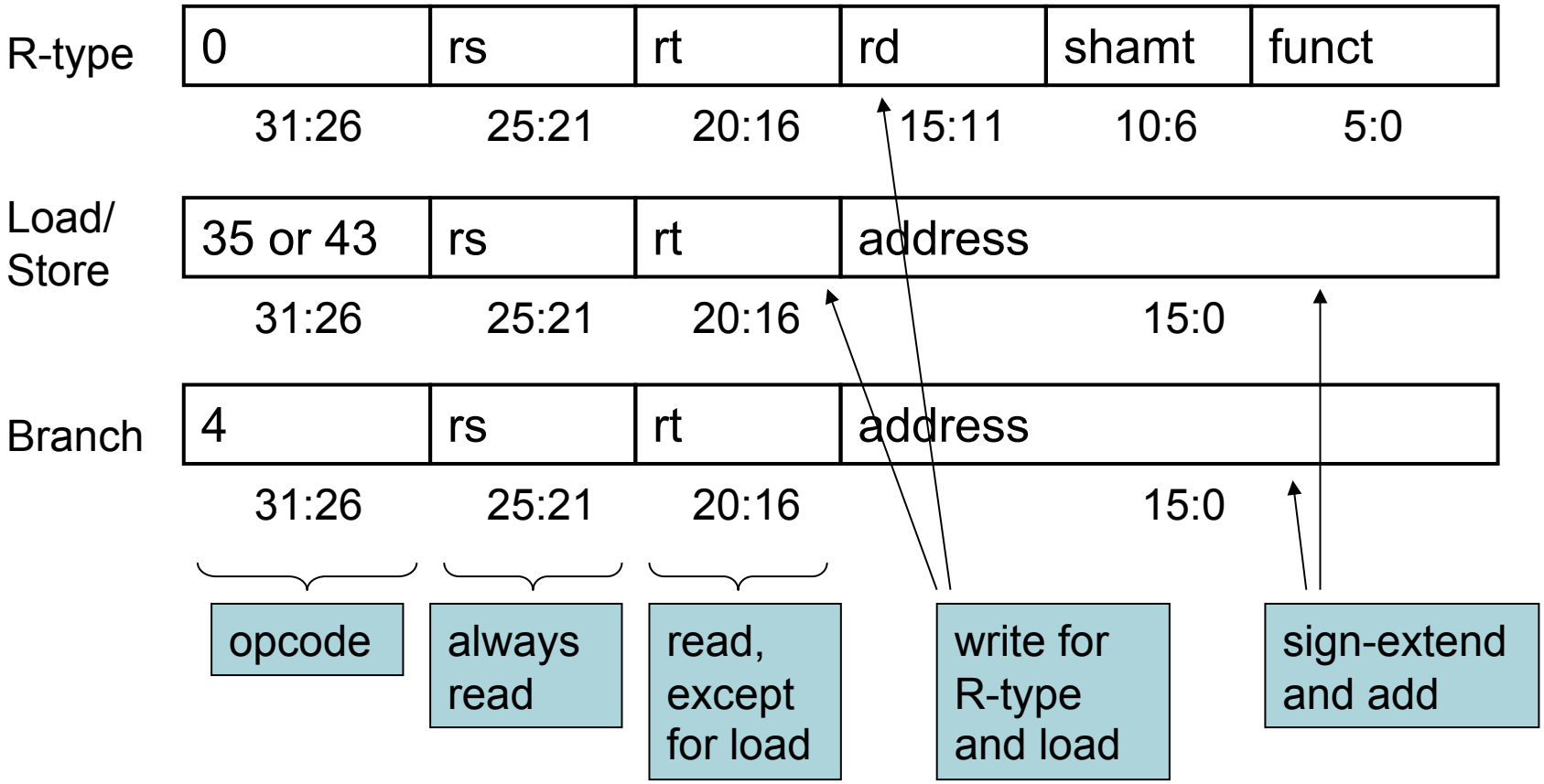
ALU control

- Assume 2-bit ALUOp derived from opcode
  - Combinational logic derives ALU control

opcode	ALUOp	Operation	funct	ALU function	ALU control
lw	00	load word	XXXXXX	add	0010
sw	00	store word	XXXXXX	add	0010
beq	01	branch equal	XXXXXX	subtract	0110
R-type	10	add	100000	add	0010
		subtract	100010	subtract	0110
		AND	100100	AND	0000
		OR	100101	OR	0001
		set-on-less-than	101010	set-on-less-than	0111

The main control unit

- Control signals derived from instruction



Main decoder

Instruction	$Op_{5:0}$	RegWrite	RegDst	AluSrc	Branch	Mem-read	MemWrite	MemtoReg	$ALUOp_{1:0}$
R-type	000000	1	1	0	0	0	0	0	10
`lw`	100011	1	0	1	0	1	0	0	00
`sw`	101011	0	X	1	0	0	1	X	00
`beq`	000100	0	X	0	1	0	0	X	01
`addi`	001000	1	0	1	0	0	0	0	00