EN164: Design of Computing Systems
Lecture 29: Memory Systems 5

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[ material from Jacob, Ng and Wang 1st ed]
DRAM is usually a shared resource among multiple processors, GPU and I/O devices -> a controller is need to coordinate the access
**DRAM organization (1-bit array)**

- Reads are destructive; content must be restored after reading
- Capacitors are leaky so they must be periodically refreshed
- DRAM controller must each refresh each row (by reading and re-writing it) every 64 ms or less
- Refreshing contributes to the slow access of DRAMs
In a x4 DRAM part, four arrays each read 1 data bit in unison, and the part sends out 4 bits of data each time the memory controller makes a column read request.
DRAM operation: bus transmission
DRAM operation: row access
DRAM operation: column access
DRAM operation: data transfer
DRAM operation: bus transmission
Simple asynchronous memory reading

Lower pin count (cost) by using same pins for row and column addresses
To increase throughput, SDRAM outputs the data of sequential columns of the same row into the data bus (BURST mode). Now needs a clock.

- Matches well with cache blocks with multiple bytes
Transfer data on positive and negative edges of the clock
DRAM memory bus organization

Word address  | Bank 0 | Word address  | Bank 1 | Word address  | Bank 2 | Word address  | Bank 3
---|---|---|---|---|---|---|---
0 |  | 1 |  | 2 |  | 3 |  
4 |  | 5 |  | 6 |  | 7 |  
8 |  | 9 |  | 10 |  | 11 |  
12 |  | 13 |  | 14 |  | 15 |  

bank
Memory interleaving

- **4-word wide memory**
  - Miss penalty = 1 + 15 + 1 = 17 bus cycles
  - Bandwidth = 16 bytes / 17 cycles = 0.94 B/cycle

- **4-bank interleaved memory**
  - Miss penalty = 1 + 15 + 4×1 = 20 bus cycles
  - Bandwidth = 16 bytes / 20 cycles = 0.8 B/cycle
DRAM connections

In PC

In smart phones/tablets

DRAM die

Processor die

A PoP implementation

Lower density I/O BGA ball count (0.65mm pitch and more) connects memory die to landing pads on the top of the bottom package. Memory die typically require less I/O than logic die

Stacked memory die

Gold or copper wirebonds

Single or multiple ASIC logic die

Laminate substrate (essentially a mini PCB)