

1. [30 points] The following core is written in C, where elements within the same row are stored contiguously

```
for (J = 0; J < 8000; J++)  
    for (I = 0; I < 8; I++)  
        A[I][J] = B[I][0] + A[J][I];
```

- [5 points] How many 32-bit integers can be stored in a 16-byte cache line?
- [5 points] References to which variables exhibit temporal locality?
- [5 points] References to which variables exhibit spatial locality?

Locality is affected by both the reference order and data layout. The same computation can also be written below in Matlab, which differs from C by contiguously storing matrix elements within the same column.

```
for J = 1:8000  
    for I = 1:8  
        A(I, J) = B(I, 0) + A(J, I);  
    end  
end
```

- [5 points] How many 16-byte cache lines are needed to store all 32-bit matrix elements being referenced?
- [5 points] References to which variables exhibit temporal locality?
- [5 points] References to which variables exhibit spatial locality?

2. [30 points] For a direct-mapped cache design with 32-bit address, the following bits of the address are used to access the cache. Tag: 31-12, Index: 11-6, and Offset: 5-0.

- [5 points] What is the cache line size (in words)?
- [5 points] How many entries does the cache have?
- [5 points] What is the ratio between the total bits required for such a cache implementation over the data storage bits?

Starting from the power on, the following byte-addressed cache references are recorded
Address: 0, 4, 16, 132, 232, 160, 1024, 30, 140, 3100, 180, 2180.

- d. [5 points] How many blocks are replaced?
- e. [5 points] What is the hit ratio?
- f. [5 points] List the final state of the cache, with each valid entry represented as a record of <index, tag, data>.

3. [15 points] Assume the following address stream:

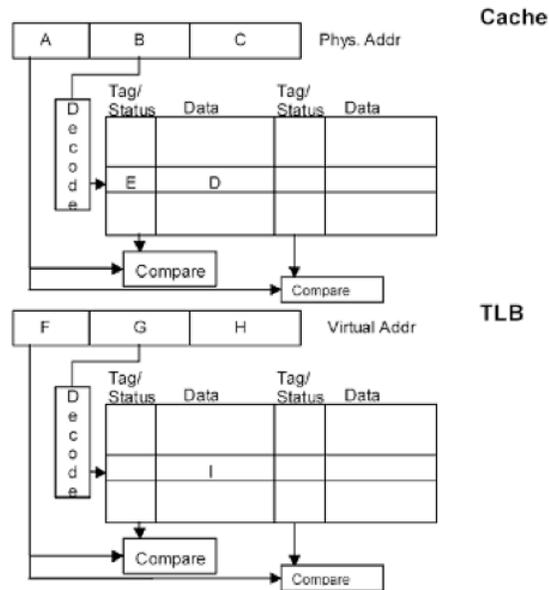
3, 180, 43, 2, 191, 88, 190, 14, 181, 44, 186, 253

- a. [5 points] Show the final cache contents for a three-way set associate cache with two-word blocks and a total size of 24 words. Use the LRU replacement. For each reference identify the index bits, the tag bits, the block offset bits, and if it is a hit or a miss.
- b. [5 points] Show the final cache contents for a fully associate cache with one-word blocks and a total size of 8 words. Use LRU replacement. For each reference, identify the index bits, the tag bits, and if it is a hit or a miss.
- c. [5 points] What is the miss rate for a fully associate cache with two-word blocks and a total size of 8 words, using LRU replacement? What is the miss rate using MRU (most recently used) replacement? Finally what is the best possible miss rate for this cache, given any replacement policy?

4. [25 points] A x16 DRAM device has a total capacity of 128 KB (kilobytes). Assume that the memory array is square in size.

- a. What is the size of the row decoder?
- b. What is the size of the column decoder?
- c. What is the number of output data bits?
- d. Assume you have a number of these DRAM devices available. Explain, with diagrams, how to connect these devices to create a memory system of total capacity of 1 MB with a data bus of 32 bits. Make sure to show the connections of the address bus to the DRAM devices. What is the address subspace that is covered by each device?

5. [10 points] Consider a memory system with the following parameters:
- Translation Lookaside Buffer has 512 entries and is 2-way set associative.
 - 64Kbyte L1 Data Cache has 128 byte lines and is also 2-way set associative.
 - Virtual addresses are 64-bits and physical addresses are 32 bits.
 - 8KB page size
- Below are diagrams of the cache and TLB. Please fill in the appropriate information in the table that follows the diagrams:



L1 Cache			TLB		
A =		bits	F =		Bits
B =		bits	G =		Bits
C =		bits	H =		Bits
D =		bits	I =		Bits
E =		bits			

6. [10 points] There are several parameters that impact the overall size of the page table. Listed below are several key page table parameters.

Virtual address size: 32 bits
 Page size: 4 KB (kilobyte)
 Page Table Entry Size (4 bytes)

- a. [5 points] Calculate the total page table size for a system running 5 applications that utilize half of the memory available.
- b. [5 points] A cache designer wants to increase the size of a 4 KB virtually indexed, physically tagged cache. Given the page size parameter above, is it possible to make a 16 KB direct-mapped cache assuming 2 words per block? How would the designer increase the data size of the cache?