Brown University
School of Engineering
EN1640 Design of Computing Systems
Professor Sherief Reda
HW 02. 50 points. Due Date: Tuesday, March 18th in class.

1. [10 points]
   a. [2 points] Assume a single-cycle processor design with a clock period *S*. If the design is pipelined to *n* stages, express the clock period and frequency as a function of *n*. Assume that the delay overhead of adding a pipeline register is *h*.
   b. [8 points] If the single-cycle design has a total capacitance of *C,* what is the dynamic power consumption of the pipelined design as a function of *n*? Assume that each pipeline register adds an additional capacitance of value *a*, and that the operating voltage of the pipeline design is equal to *V*.

2. [10 points]

   a. [5 points] You are going to enhance a computer, and there are two possible improvements: either make multiply instructions run four times faster than before, or make memory access instructions run two times faster than before. You repeatedly run a program that takes 100 seconds to execute. Of this time, 20% is used for multiplication, 50% for memory access instructions, and 30% for other tasks. What is speedup if you improve only multiplication? What will the speedup be if you improve only memory access? What is the speedup if both improvements are made?

   b. [5 points] You are going to change the program described in (a) so that the percentages are not 20%, 50%, and 30% anymore. Assuming that none of the new percentages is 0, what sort of program would result in a tie (with regard to speedup) between the two individual improvements? Provide both a formula and some examples.

3. [10 points] Suppose that one of the following control signals in the signals in the single-cycle MIPS processors has a stuck-at-0 fault, meaning that the signal is always 0 regardless of its intended value. What instructions would malfunction? Why?
   a) RegWrite
   b) $ALUop_1$
   c) MemWrite

4. [10 points] Many processor architectures have a load with post-increment instruction, which updates the index register to point to the next memory word after completing the load. `lwinc $rt, imm($rs)` is equivalent to the following two instructions:

```
lw $rt, imm($rs)
addi $rs, $rs, 4
```

Modify the single-cycle MIPS processor to implement the `lwinc` instructions. Sketch the datapath indicating the changes compared to the datapath given in the lecture, and name any control signals as well changes to the decoder.

5. [10 points] Assume the following datapath latencies for the individual stages.

IF: 250 ps
ID: 350 ps
EX: 150 ps
MEM: 300 ps
WB: 200 ps

a. [2 points] What is the clock cycle time in a pipelined and non-pipelined processor?
b. [3 points] What is the total latency of an LW instruction in a pipelined and non-pipelined processor? Ignore the overhead of the pipeline registers.
c. [5 points] If we can split one stage of the pipelined datapath into two new stages, each with half the latency of the original stage, which stage would you split and what is the new clock cycle time of the processor?