

1. [15 points]

I1:	LW	R1, 0 (R1)
I2:	AND	R1, R1, R2
I3:	LW	R2, 0 (R1)
I4:	LW	R1, 0 (R3)

- [5 points] Find all data dependences in this instruction sequence.
- [5 points] Find all hazards in this instruction sequence for a 5-stage pipeline with and then without forwarding
- [5 points] To reduce clock cycle time, we are considering a split of the MEM stage into two stages, where reading completes in the second MEM stage. Repeat parts (a) and (b) for this 6-stage pipeline

2. [25 points] The pipelined MIPS processor is running the following program.

```
add    $t0, $t0, $t1
sub    $s1, $t2, $t3
and    $s2, $s0, $s1
or     $s3, $t4, $t5
slt    $s4, $s2, $s3
```

- [5 points] Which registers are being written, and which are being read in the sixth clock cycle?
- [5 points] Identify all Read After Write (RAW) hazards.
- [5 points] Modify the program to eliminate the hazards by inserting nop instructions in the program to eliminate any RAW hazards. How many cycles does it need to complete the modified program?
- [5 points] Reorder the instructions in the program, while maintaining correctness, to eliminate the RAW hazards. How many cycles does it need to complete the modified program?
- [5 points] Explain how a hazard detection unit can eliminate the RAW hazards in the program without the need for software modifications. Comment on the incurred costs of using a hazard detection unit with forwarding.