Brown University
School of Engineering
EN164 Design of Computing Systems
Professor Sherief Reda
HW 05. 50 points. Due Date: Tuesday, April 21th in class.

1. (10 points) Suppose you are running a program that is attempting to load words from the following addresses. The address pattern is executed only once.

   0x0, 0x8, 0x10, 0x18, 0x20, 0x28

(a) If you use direct mapped cache with cache size 1 KB and a block size of 8 bytes (two words), how many sets (i.e., lines) are in the cache?

(b) With the same cache and block size as in part (a), what is the miss rate of the direct mapped cache for the given memory access pattern?

(c) For the given memory access pattern, which of the following would decrease the miss rate the most? (Cache capacity is kept constant). Circle one
   i. Increasing the degree of associativity to 2
   ii. Increasing the block size to 16 bytes
   iii. Either (i) or (ii)
   iv. Neither (i) nor (ii)

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2. (30 points) Most scientific applications involve matrix operations. The most common operation is matrix multiply: X=YZ, where X, Y, and Z are *N*-by-N matrices. Assume that the elements of X are computed row-by-row, and matrix sizes are 256 × 256. Each element is a double precision floating-point number (8 bytes). Assume a fully associative data cache with a least recently used (LRU) replacement policy. Assume a total cache size of 128 KB and that the cache block size is 8 bytes as well and that operands are aligned.

   a. Compute the total number of misses in the data cache. To compute the data cache miss rate, we neglect all integer access in the program execution and focus on the floating-point accesses. Also compute the total number of operations (FP ADDs and FP Mult).

   b. To reduce the miss rate, it is possible to block the matrix multiply into operations on submatricies of size *N/k* by *N/k* (*k* is power of 2). The miss rate and the execution time should improve because several submatricies easily fit in the cache now. Describe the block algorithm that should be implemented to minimize the number of misses, and compute the overall number of misses. Also compute the total number of operations (FP ADDs and FP Mult)

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3. [10 points] A x16 DRAM device has a total capacity of 128 KB (kilobytes). Assume that the memory array is square in size.

a. What is the size of the row decoder?

b. What is the size of the column decoder?

c. What is the number of output data bits?

d. Assume you have a number of these DRAM devices available. Explain, with diagrams, how to connect these devices to create a memory system of total capacity of 1 MB with a data bus of 32 bits. Make sure to show the connections of the address bus to the DRAM devices. What is the address subspace that is covered by each device?
