Brown University
School of Engineering
EN164 Design of Computing Systems
Professor Sherief Reda
HW 06. 50 points. Due Date: Tuesday, April 29th in class.

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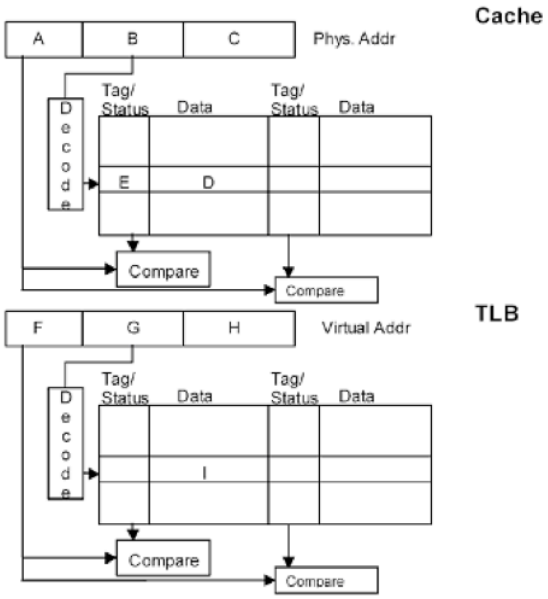
1. [15 points] Consider a memory system with the following parameters:
   - Translation Lookaside Buffer has 512 entries and is 2-way set associative.
   - 64Kbyte L1 Data Cache has 128 byte lines and is also 2-way set associative.
   - Virtual addresses are 64-bits and physical addresses are 32 bits.
   - 8KB page size Below are diagrams of the cache and TLB. Please fill in the appropriate information in the table that follows the diagrams:



L1 Cache		TLB	
A =	bits	F =	Bits
B =	bits	G =	Bits
C =	bits	H =	Bits
D =	bits	I =	Bits
E =	bits		

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2. [15 points] There are several parameters that impact the overall size of the page table. Listed below are several key page table parameters.

Virtual address size: 32 bits
Page size: 4 KB (kilobyte)
Page Table Entry Size (4 bytes)

a. Calculate the total page table size for a system running 5 applications that utilize half of the memory available.

b. A cache designer wants to increase the size of a 4 KB virtually indexed, physically tagged cache. Given the page size parameter above, is it possible to make a 16 KB direct-mapped cache assuming 2 words per block? How would the designer increase the data size of the cache?

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3. [10 points] Communicating with I/O devices is achieved using combinations of polling, interrupt handing, memory mapping and special I/O command. Specific I/O commands are a mode of I/O communication in which specific instruction (e.g., `in` and `out`) Answer the following questions about communicating with I/O subsystems for the following applications using combinations of these techniques

a. Auto Pilot
b. Automated thermostat

1. Describe device polling. Would each application in the table be appropriate for communication using polling techniques? Explain.
2. Describe interrupt driven communication. For each application in the table, if polling is inappropriate, explain how interrupt driven techniques could be used.
3. For the applications listed in the table, outline a design for memory mapped communication. Identify reserved memory locations and outline their contents.

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4. [10 points] Direct Memory Access (DMA) allows devices to access memory directly rather than working through the CPU. This can dramatically speed up the performance of peripherals, but adds complexity to memory system implementations. Explore DMA implications by answering the questions about the following peripherals

a. Mouse controller
b. Ethernet controller

1. Does the CPU relinquish control of memory when DMA is active? For example, can a peripheral simply communicate with memory directly, avoiding the CPU completely?
2. Of the peripherals listed in the table, which would benefit from DMA? What criteria determine if DMA is appropriate?
3. Of the peripherals listed in the table, which could cause coherency problems with cache contents? What criteria determine if coherency issues must be addressed?
4. Describe what problems could occur when mixing DMA and virtual memory. Which of the peripherals in the table could introduce such problems? How can they be avoided?