Brown University
School of Engineering
ENGN1640 Design of Computing Systems
Professor Sherief Reda
LAB 02 (50 points).
Due in lab to TA by Friday, Feb 21.

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Please follow Tutorial 3 (SignalTap tutorial) before you work on these labs.

In the first lab you explored combinational designs. This lab requires you to design sequential designs. For your lab report, please make sure to report (1) the total logic and routing resources utilized by your circuit; (2) a screen capture of your schematic; (3) a screen capture of the RTL circuit view (tools → netlist viewer → RTL viewer); (4) a screen capture of the post-mapped circuit view (tools → netlist viewer → technology map); (5) a screen capture for the floorplan after fitting; (6) functional simulation waveforms; and (7) timing simulation waveforms. You are allowed to use a mix for Verilog and schematics for the exercises, but your Verilog code should form at least "80%" of your designs. For these designs, you will have to use the available 50 Mhz clock signal to create the required period.

(1) (25 points) Design a light blinker that flashes a red LED. When first programmed, the LED should have a period of 0.5 second (i.e., on for 0.25 seconds, off for 0.25 seconds). Every time the user presses the first blue key, the period should be doubled. Use the signalTap tool to capture a sample of the changes in your internal states of your flipflops and include a screenshot. Report the additional overhead (e.g., LEs and routing) introduced by the SignalTap tool.

(2) (25 points) Design a stopwatch that counts in the tenth of a second using the 7-segment displays. You should use two digits for the minutes, two digits for the seconds, and one digit for the tenth of the second. Two push should be used. One for Start/Stop and the other one for Reset. **Make sure to optimize your design to use the fewest LEs.** [5 points of this question will be allocated based on the optimization results of correct designs]