

Brown University
School of Engineering
ENGN1640 Design of Computing Systems
Professor Sherief Reda
LAB 01 (50 points).
Due in lab to TA by Friday, Feb 19.
No collaboration on this lab is allowed.



Please make sure to follow Tutorials 1 and 2 on the class webpage before you attempt this exercise. Tutorial 2 is almost identical to tutorial 1 except that it uses Verilog instead of Schematic design.

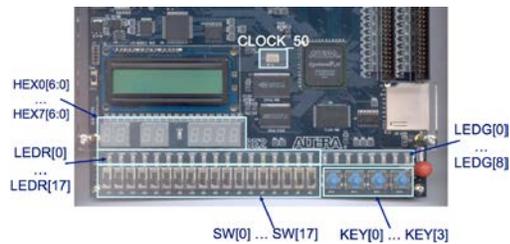
The objective of this lab is to familiarize with the Quartus II design environment and the DE2 board that hosts the FPGA. For your lab report, please make sure to report (1) the total logic and routing resources utilized by your circuit; (2) a screen capture of your schematic; (3) a screen capture of the RTL circuit view (tools → netlist viewer → RTL viewer); (4) a screen capture of the post-mapped circuit view (tools → netlist viewer → technology map); (5) a screen capture for the floorplan after fitting; (6) representative functional simulation waveforms; and (7) representative timing simulation waveforms.

- (1) (5 points) Design a circuit that only turns a red LED if the first two switches in the board are engaged; otherwise, the LED is turned off. Use only schematic entry (i.e. no Verilog) for this exercise.
- (2) (15 points) Design a module that will take a binary number of 4 bits and display the equivalent hexadecimal letter on one of the 7 segment displays. Connect the pins of the module to read the binary value from four switches on the DE2 board. Use only Verilog for this exercise.
- (3) (30 points) Design a Arithmetic Logic Unit (ALU) system that takes as inputs two 8-bit signed binary numbers (specified using the first 16 switches of the DE2 board), and the operation code (specified using two switches) and outputs the 8-bit result of the operation on the 7-segment displays. The required operations are: add, sub, multiply, and bitwise AND. A red LED should turn on if there is an overflow in the arithmetic result. You can either use Verilog alone or a mix of Verilog and schematic entry for this design. **Make sure to optimize your design to use the fewest LEs.**

10 points of question (3) will be allocated based on the optimization results of correct designs as follows:

- 10: ≤ 85 LEs, 9: ≤ 95 LEs, 8: ≤ 100 , 7: ≤ 105 , 6: ≤ 110 , 5: ≤ 120 , 4: ≤ 140 , and 3: ≤ 1000 .

Make sure to import the pin assignment from the DE2 pin assignment file (csv) that is available at the class web site. The names of various input/output signals are given in the figure below.



Helpful Tips:

- To access the floorplan, choose Tools → Chip Planner
- To access the resource utilization, choose Processing → Compilation Report
- The Quartus tool has an extensive library of pre-designed megafunctions that implement many functions (e.g., decoders, counters, registers, comparators, ROMs, etc). You should use these megafunctions whenever possible. You can access the library by clicking the “symbol tool” in the tool bar.