



Please follow Tutorial 3 on how to use MentorGraphics ModelSim before you work on these labs.

In the first lab you explored combinational designs. This lab requires you to design sequential designs. For your lab report, please make sure to report (1) the total logic and routing resources utilized by your circuit; (2) your Verilog code and your Verilog testbench for ModelSim, and (3) functional verification outcomes from ModelSim. For these designs, you will have to use the available 50 MHz clock signal to create the required period.

- (1) (25 points) Design a circuit to **compute** the Fibonacci numbers (1, 1, 2, 3, 5, 8, ...). The circuit should use a switch to enable the circuit to operate. Starting from 1, a new Fibonacci number should appear on the seven segment display (max two digits) every second. Do not use RAM/ROM to generate the Fibonacci numbers; the numbers should be computed on the fly.

- (2) (25 points) Design a stopwatch that counts in the tenth of a second using the 7-segment displays. You should use two digits for the minutes, two digits for the seconds, and one digit for the tenth of the second. Two push should be used. One for Start/Stop and the other one for Reset. **Make sure to optimize your design to use the fewest LEs.** 5 points of this question will be allocated for optimization. $5: \leq 80$, $4 \leq 90$, $3: \leq 95$, $2: \leq 100$.