Brown University
School of Engineering
EN164 Design of Computing Systems
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LAB 07 (100 points)
Final report due on Friday May 6 2016

In this lab you are going to augment the design of your processor with external memory. You can either use your single-cycle design or pipeline design as the baseline.

It is required to interface your processor to the external asynchronous 256 KB ×16 SRAM available on the FPGA board. You should use this external SRAM to substitute your internal M4K used for your data memory. The interfacing will be done by designing a memory controller that takes as inputs the original inputs to the internal memory (e.g., address bus, data bus, memory read/write control signals) and outputs a 32 bit data and potential other new control signals. Since the SRAM has a 16-bit data bus, writing or reading from the SRAM requires two bus cycles to read/write 32 bits. Implement your design and check it correctness by running the factorial program and reading the content of the external SRAM. To read the content of the external SRAM, there is a tool (DE2 control panel) that can be used to check the content of the SRAM; however, before using it, you need to download its .sof file in the FPGA. Note that this downloading does not affect the content of the SRAM because it is external to the FPGA. Report the frequency of operation, the average cycles per instruction, and the design area required for the memory controller. Contrast your design performance to the one that uses the internal M4K memory. If you were to improve your design by using the internal memory as a direct-mapped cache to the external SRAM, only explain with sketches and words (no need for implementations), how would you do the cache-based design. Please note that simulating the external memory in ModelSim might not be possible, and as a result only verification on the board is required.