ENGN 1640 Homework 01 (66 points) – Due Date: Feb 10 2016 in class

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1. [9 points] Consider three different processors P1, P2, and P3 executing the same instruction set. P1 has a 3 GHz clock rate and a CPI of 1.5. P2 has a 2.5 GHz clock rate and a CPI of 1.0. P3 has a 4.0 GHz clock rate and has a CPI of 2.2.

   a. (3 pts) Which processor has the highest performance expressed in instructions per second?

   b. (3 pts) If the processors each execute a program in 10 seconds, find the number of cycles and the number of instructions.

   c. (3 pts) We are trying to reduce the execution time by 30% but this leads to an increase of 20% in the CPI. What clock rate should we have to get this time reduction?

2. [13 points] Consider two possible improvements for a base machine: one improving floating point performance and one improving memory performance. Three programs are simulated: one with no floating-point operations (Program 1), one dominated by floating-point operations (Program 2), and one with balance between memory accesses and floating-point operations (Program 3). The execution time of each program on the three machines is given in the following table.

Machines	Program 1	Program 2	Program 3
Base machine	1 s	10 ms	10 s
Base + FP units	1 s	2 ms	6 s
Base + cache	0.7 s	9 ms	5 s

   a. (3 pts) Calculate the average execution time for each machine. Which machine is better?

   b. (10 pts) Compared to the base machine, calculate (i) arithmetic means of speedup and (ii) geometric means of speed. Which machine is better? Please explain any discrepancy to the conclusion compared to question (a).

3. [4 points] In machine M1, which is clocked at 100 MHz, it was observed that 20% of the computation time of the integer benchmarks is spent in a subroutine $multiply(A,B,C)$, which multiplies integer A and B and returns the result in C. Furthermore, each invocation of $multiply$ takes 800 cycles to execute. To speed up the program it is proposed to introduce a new machine, M2, with a special native instruction MULT, where MULT takes 40 cycles. Besides the multiplies all other instructions take the same number of cycles. Because of the added complexity, however, the clock rate of M2 is only 80 MHz. How much faster or slower is M2 compared to M1?

4. [10 points] The Pentium 4 Prescott processor, released in 2005, had a clock rate of 3.6 GHz and voltage of 1.25 V. Assume that, on average, it consumed 10 W of static power and 90 W of dynamic power. Static power, sometimes is called leakage, is consumed independent of switching activity, and it is equal to the operational voltage multiplied by the leakage current. Static power is basically waste; however, it has been increased in magnitude in recent technologies to shrinking transistor sizes. The Core i5 Ivy Bridge, released in 1012, had a clock rate of 3.4 GHz and voltage of 0.9 V. Assume that on average it consumed 30 W of static power and 40 W of dynamic power.

a. (2 pts) For each processor find the average capacitive loads.

b. (2 pts) Find the percentage of the total dissipated power comprised by the static power and the ratio of static power to dynamic power for each technology.

c. (6 pts) If the total dissipated power is to be reduced by 10%, how much should the voltage be reduced to maintain the same leakage current? Solve this question for both processors.

5. [8 points] The yield of a wafer, i.e., the fraction of good dies, is determined by the defects per unit area and the die area through the following empirical formula

$$\text{yield} = \frac{1}{(1 + (\text{Defects per area} \times \text{Die area}/2))^2}. \quad (1)$$

Assume a 15 cm diameter wafer has a cost of 12, contains 84 dies, and has 0.02 defects/cm^2. Assume a 20 cm diameter wafer has a cost of 15, contains 100 dies, and has 0.031 defects/cm^2.

a. (2 pts) Find the yield for both wafers.

b. (2 pts) Find the cost per good die for both wafers.

c. (4 pts) Assume a fabrication process improves the yield from 0.92 to 0.95. Find the defects per area unit for each version of the technology given a die area of 200 mm^2.

6. [12 points] Moore's law is showing its age! The latest Intel processors (Skylake Family) use CMOS (i.e., Complementary Metal Oxide Semiconductor) feature sizes of 14 nm. Current miniaturization trends cannot continue forever; we cannot beat physics (or death!). With the eventual demise of Moore's law on the horizon, there is a movement to continue the historic trend of increasing integration and functionality through other means. In this open-ended assignment, you are asked to use your favorite search engine to investigate some of the "More-than-Moore" technologies that are being entertained for the long-term future. Is their life beyond Moore's Law? Are there alternatives? List the three potential technologies and summarize, in your own words, their potential use and impact. Make sure to cite your references!