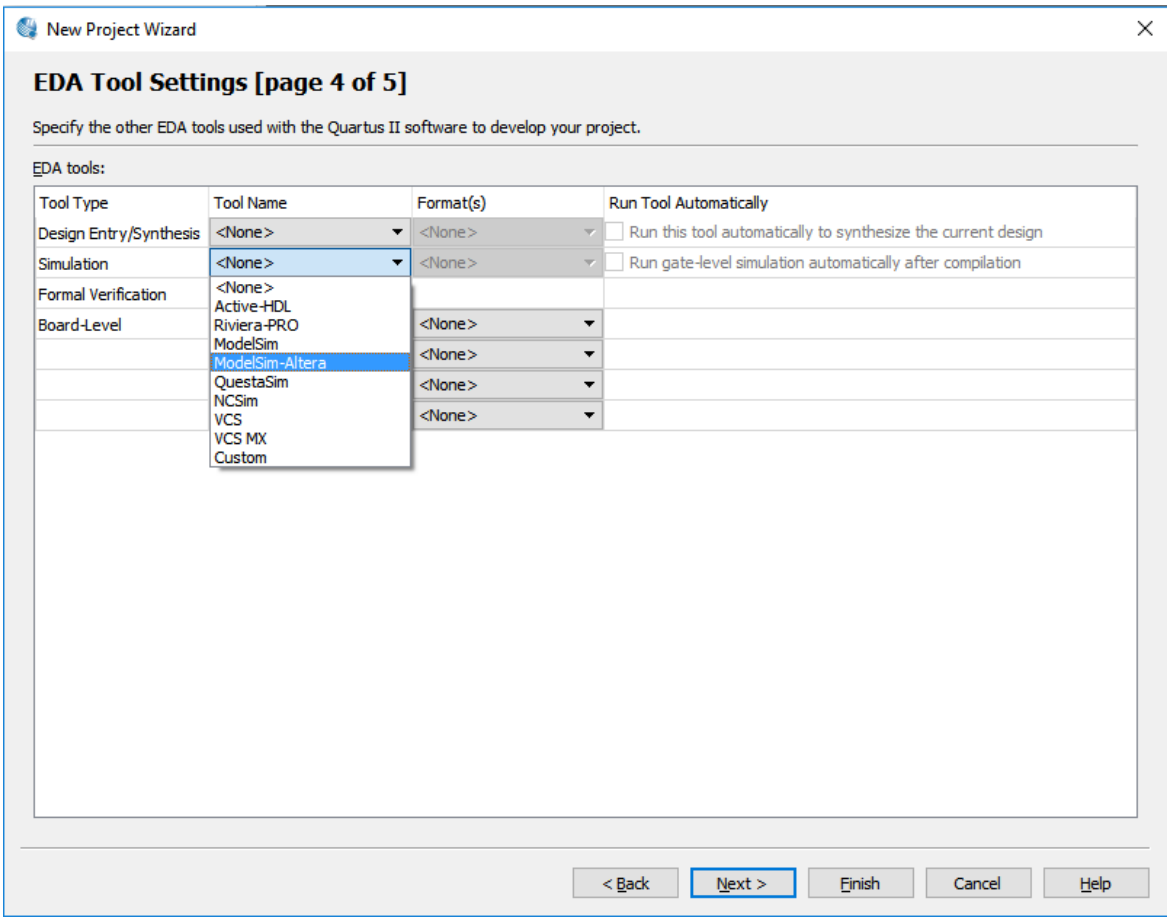
ModelSim Altera Tutorial

Start a new Quartus Project using the Project Wizard and choose **sums** as the name of design and top module; in Step 4/5 of the project creation**, make sure to select "ModelSim Altera Edition" as your simulation tool.**



Create the sums.v file for your design and use this simple code for it.

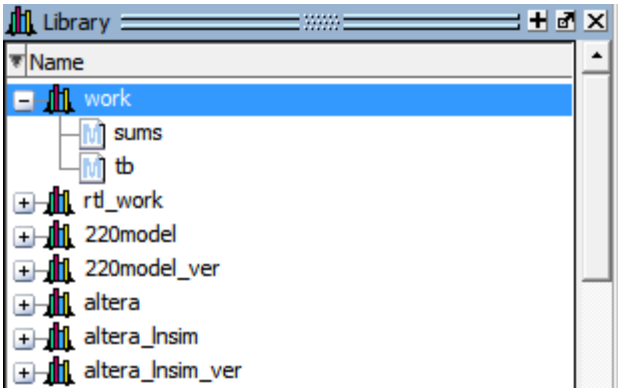
```
module sums(input clk, input [7:0] a, input[7:0] b, output reg [7:0] c);
initial
	c = 0;
always @(posedge clk)
	c <= a + b;
endmodule
```

You can compile the code to make sure there are no errors, but it is not really required if you just want to do functional simulation with ModelSim. Next you should create your testbench (I am using here one similar to the one I gave in class. Save this testbench as tb.v

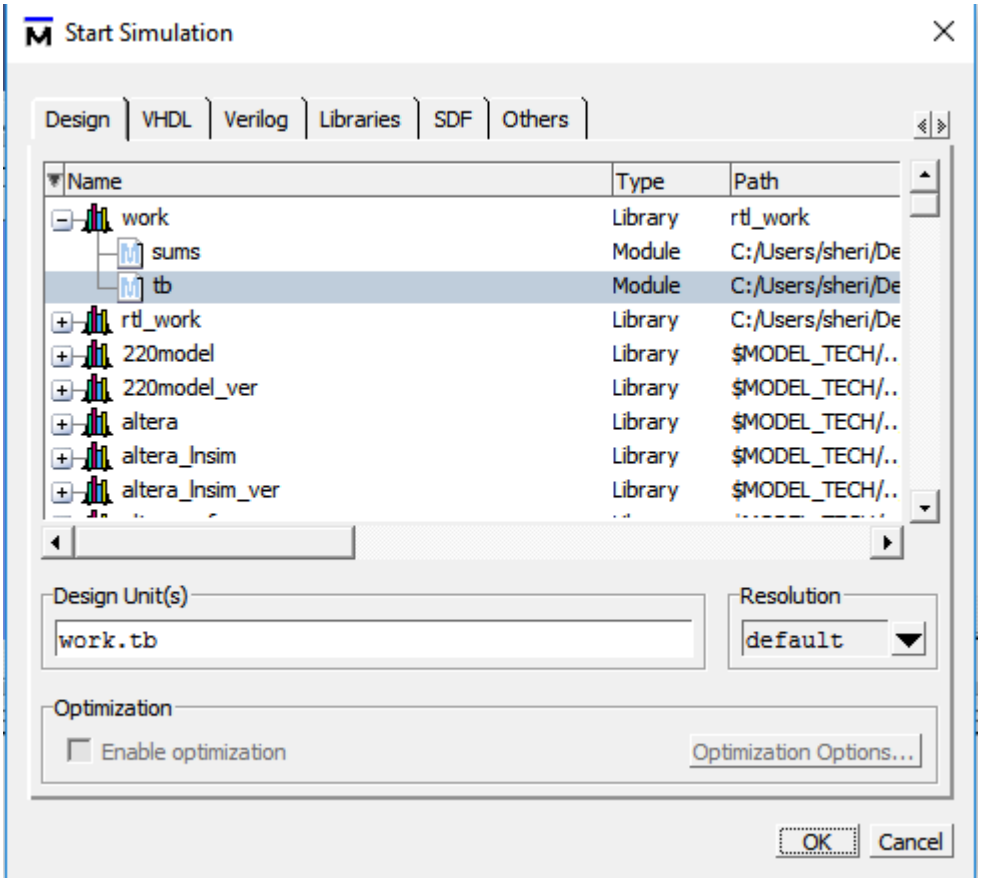
```
`timescale 10ns/1ns
module tb;
  reg [7:0] a;
  reg [7:0] b;
  reg clk;
  wire [7:0] c;

  sums s1(clk, a, b, c);
  initial
  begin
      clk = 0;
    #5 b = 20;
    #10 b = 50;
    $monitor("%d+%d=%d", a, b, c);
    #100 $stop;
  end

  always
    #10 a=$random;
  always
    #5  clk=~clk;

  always
   #10 if(c %2 == 0)
      $display("even\n");
endmodule
```

Now Launch ModelSim from Quartus: from Tools → Run Simulation Tool.

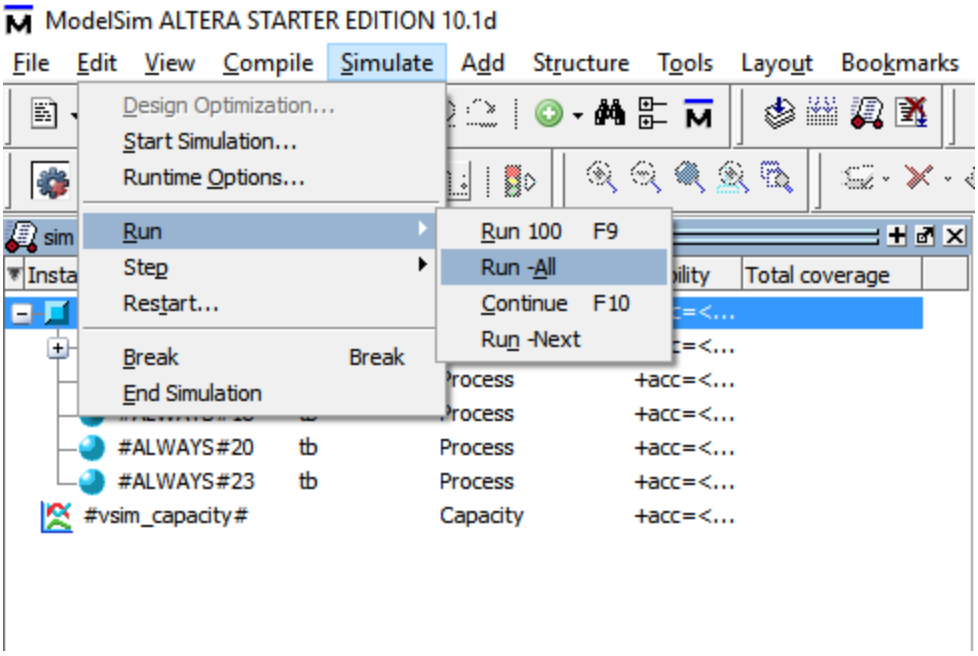
Once launched, you will see the sums module under the work library. You should then select Compile from the menu and choose the tb.v file. It will be compiled and added to the library.



Now click Simulate → start simulation, and the dialog box will open up and choose tb to simulate

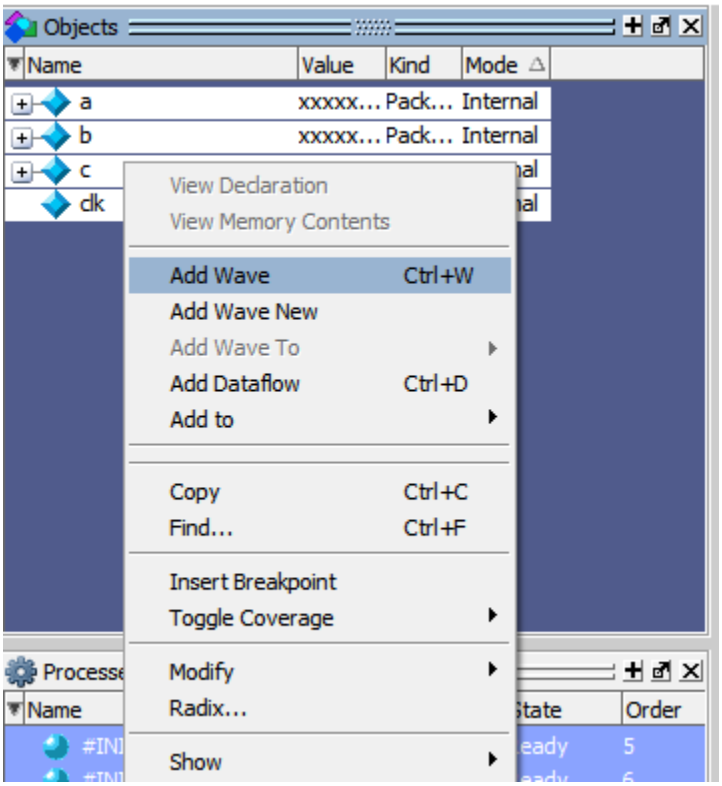


Now Run the simulation

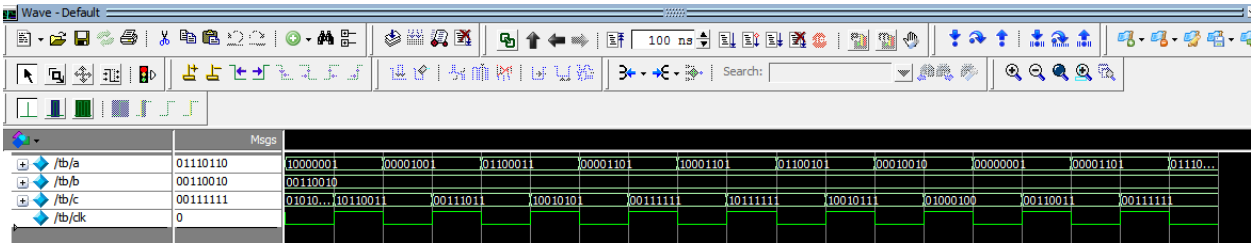


When completed, the output of the simulation will be available in the transcript window! It is that easy!

If you would like to see waveforms in addition to the text in the transcript window then you should add the desired signals as waves from the Object Window.

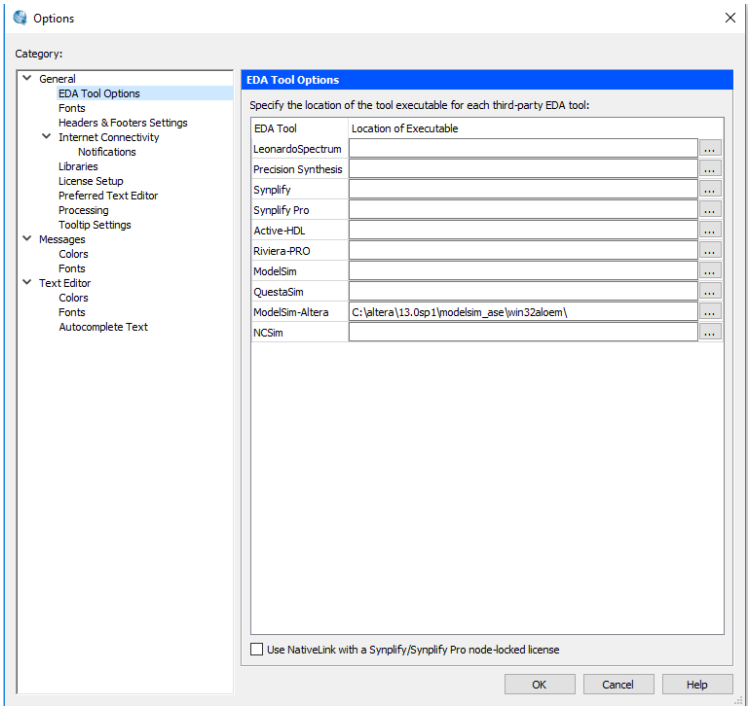


A new window will launch and then Run again and now you will get waveforms in addition to the text output

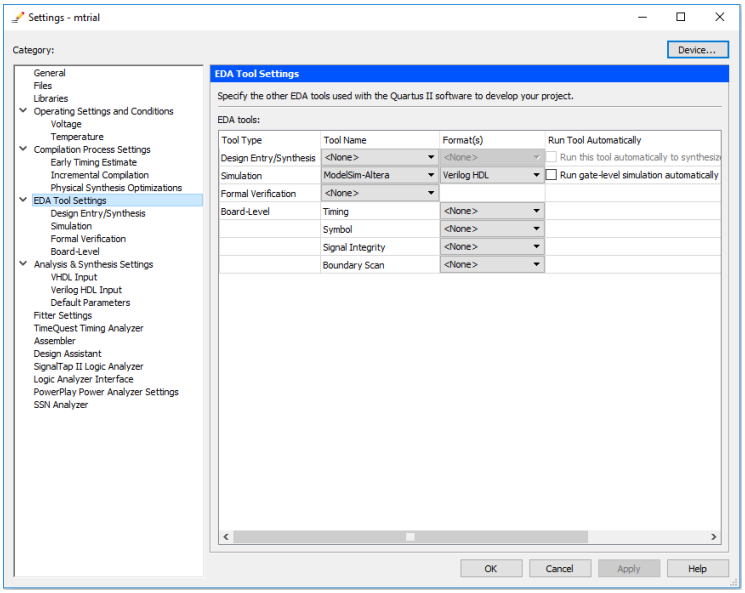


Steps to make sure Builtin modules and timing simulation is done correctly

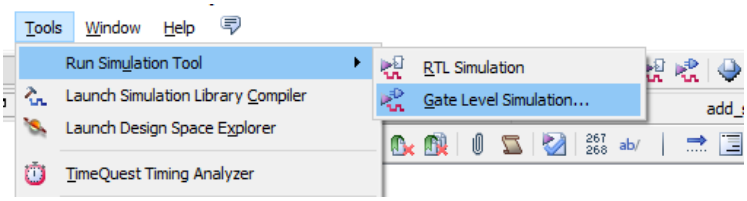
1. First, make sure that Options→Tools has the right path to the ModelSim executable



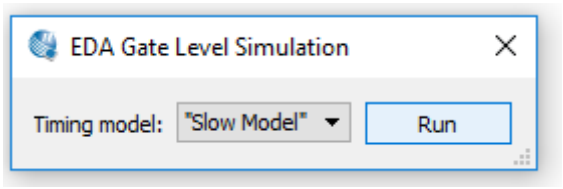
2. And that ModelSim-Altera Verilog is your simulator (you probably did this any way before)



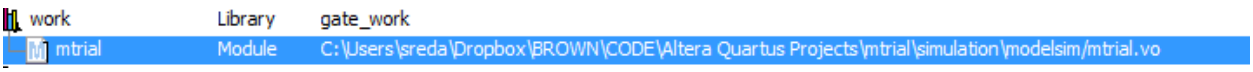
3. After you compile your code, select Tools and choose gate-level simulation



4. You can choose the slow or fast models



5. You should now notice that the module included in the library is pointing to a .vo file instead of v. This is a right sign as the .vo will include this information to model Altera modules and the timing information.



6. Step 6 is as in the regular case as you need to compile your testbench into the library.

7. When you now click start simulation, make sure to choose the libraries tab and choose the following two libraries and then select the testbench from the Design tab and press OK. The rest of the simulation is business as usual.