ENGN1640: Design of Computing Systems

Topic 00: Class Overview

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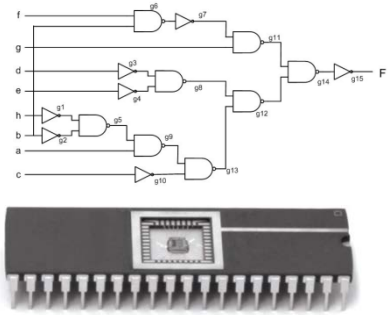
Spring 2017

Custom versus Programmable HW

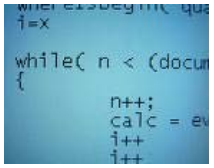
ENGN 1630: Hardware (Application Specific Integrated Circuits)



Advantages:
- very high performance and efficient

Disadvantages:
- not flexible (can't be altered after fabrication)
- expensive

ENGN1640: Software-programmed processors



Advantages:
- Hardware can run man programs
- software is very flexible to change

Disadvantages:
- performance can suffer
- fixed instruction set by hardware

Computing systems in general







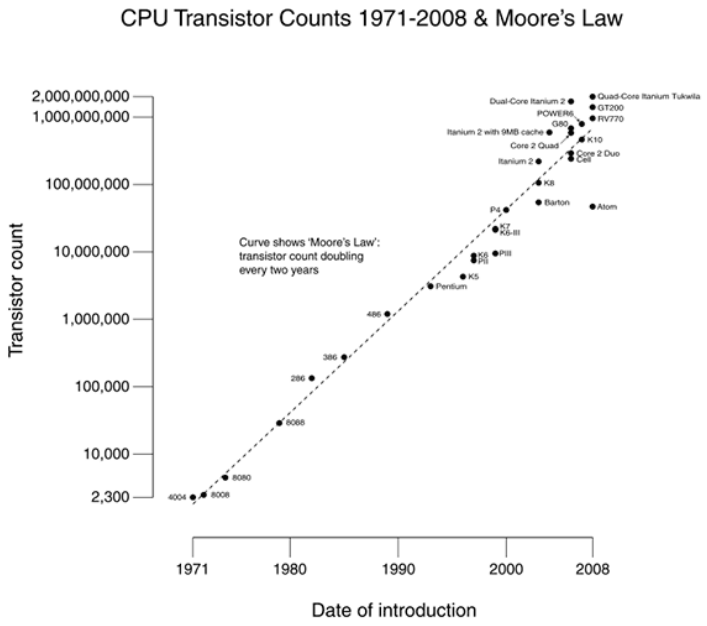

- Computing has evolved from its mainframe and personal origins to being embedded and ubiquitous.

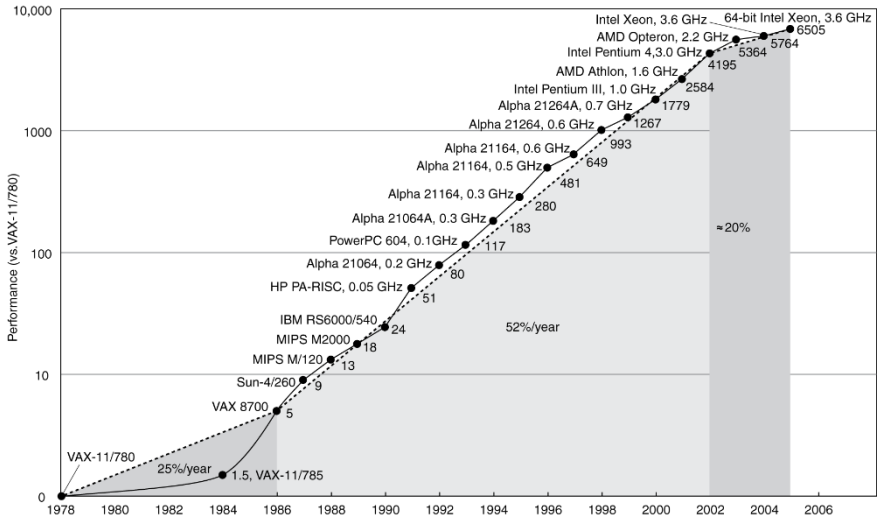
Objectives of computing system design

- Performance
- Power
- Cost
- Flexibility
- Reliable
- Secure

Exact design objectives depend on the context and intended field of deployment

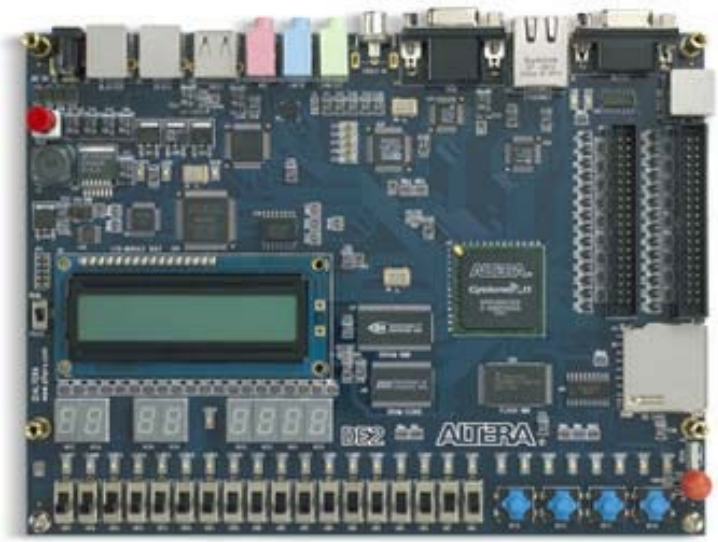
Topic 01. Introduction





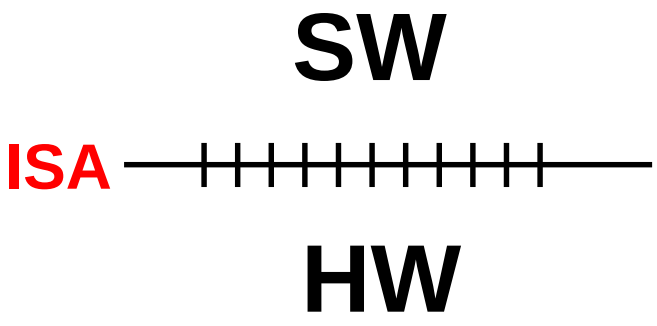
1. Evaluating computing systems: performance, power, cost
2. Trends and current bottlenecks in computing

Topic 02. FPGAs and HDL for labs



- Learn basics of programmable logic
- Learn how to use design and simulation tools
- Learn a popular hardware definition language (HDL) Verilog
- Lab incorporated in most class topics

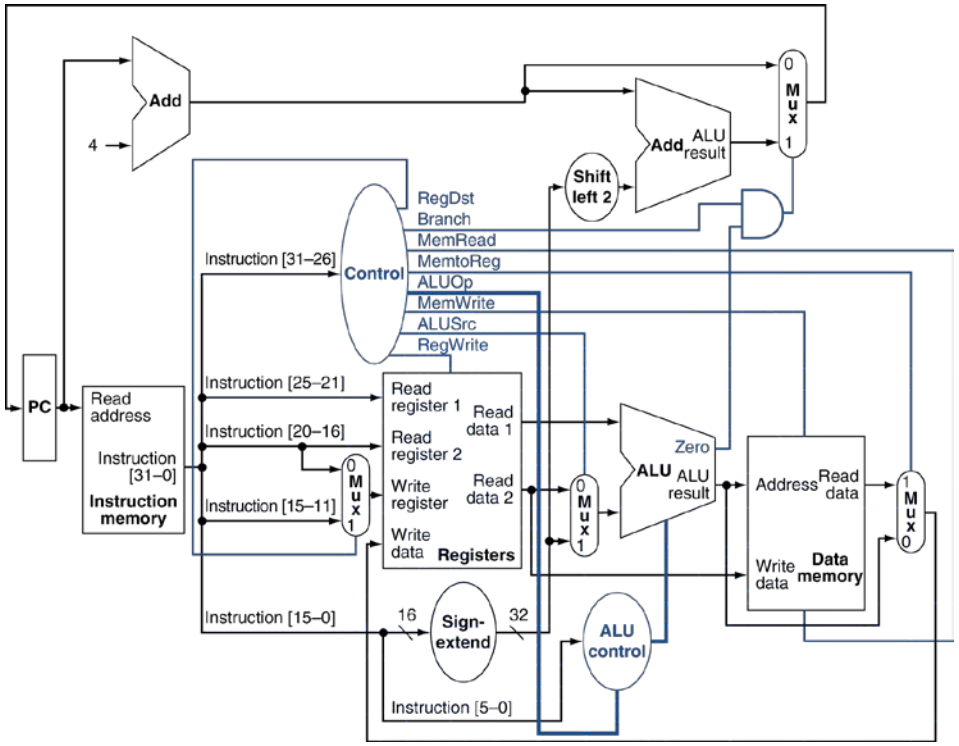
Topic 03. Instruction Set Architecture




```
lw  $t0, 32($s3)
add $t0, $s2, $t0
sw  $t0, 48($s3)
store word
```

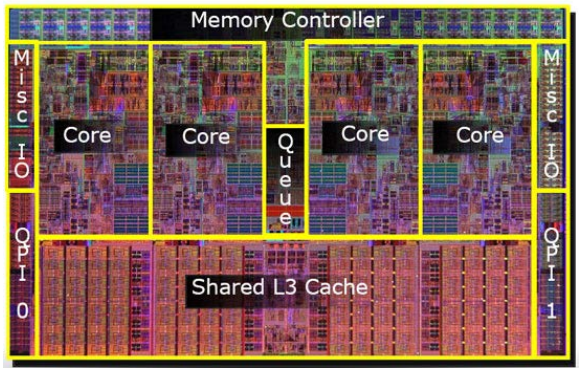
- Instruction set architecture design (ISA) choices
- Principles of instruction set design
- ISA classifications and trade-offs
- Encoding and assembly language
- Examples of assembly languages

Topic 04. Processor Design (ARMv4)

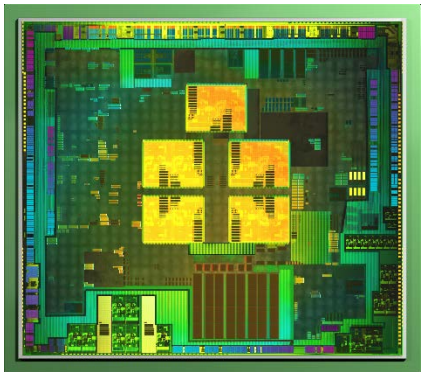


- Scalar processor design
- Pipelined processor design
- Hazards and hazard elimination techniques
- Labs will develop and boot a real processor

Topic 05. Advanced processor design



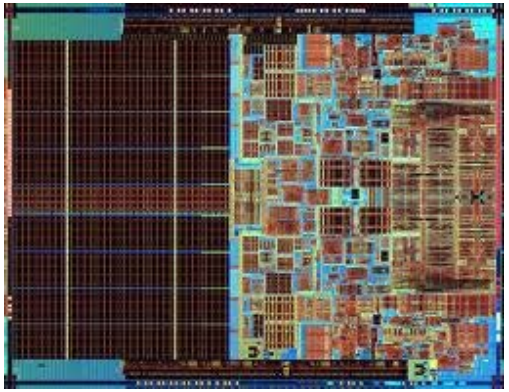
Intel Core i7


NVIDIA Tegra 3 SoC


Clusters

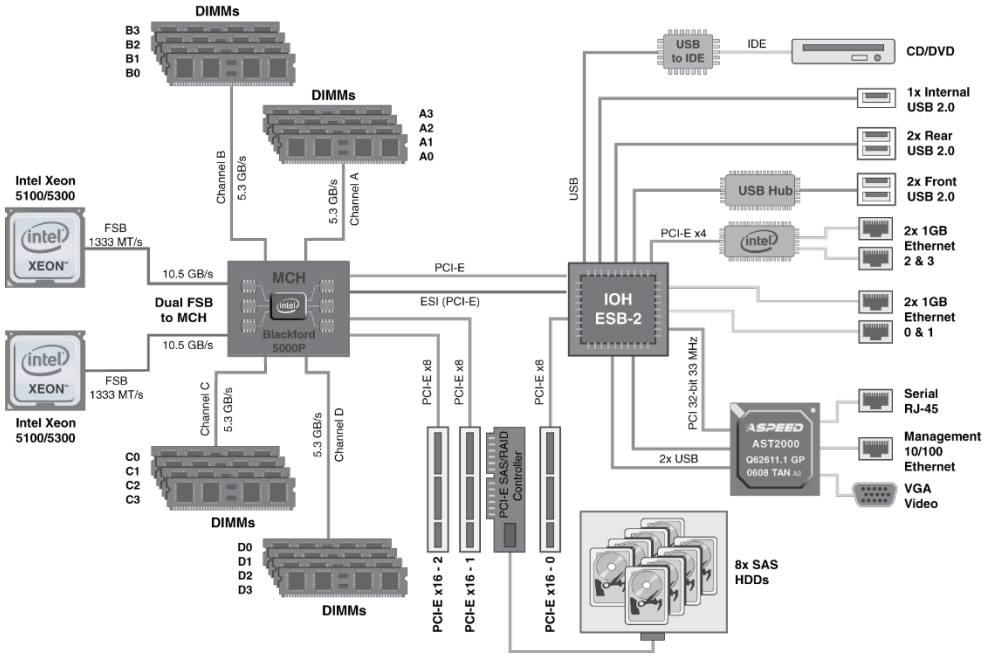
- Vector instructions
- Superscalar processors
- Multi-threading and multi-core processors

Topic 06. Memory hierarchy



- Memory hierarchy design
- Cache memory organizations
- Memory technologies: SRAM (cache), DRAM, Flash
- Virtual memory

Topic 07. Input / Output



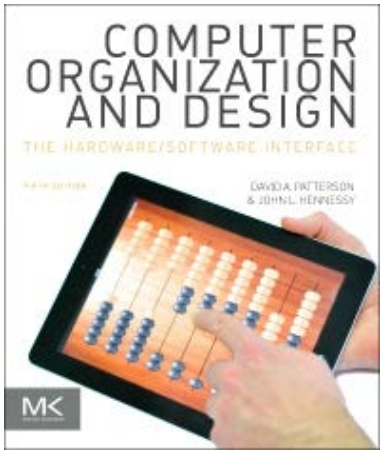
- Communication between processor, memory and I/O devices
- Interrupts and interrupt handling
- Direct Memory transfer

Prerequisites & books

Prerequisites:

- ENGN1630: digital logic design: binary numbers, combinational circuits, arithmetic circuits, sequential circuits.
- Or Pass the digital logic evaluation quiz

Course Book:



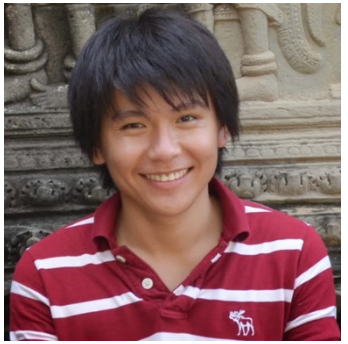
[5th edition]

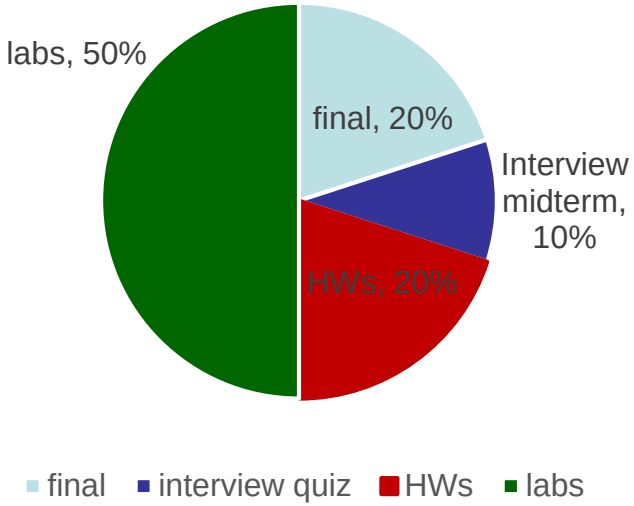
Website: http://scale.engin.brown.edu/classes/EN164S17/

Grading and logistics

- **Grading philosophy**: class is about design and better designs should get higher grades.
- HWs are always due on Wednesdays in class. 1 student / HW.
- Labs are always due on Fridays. 1 or 2 student per Lab problem.
- HW or lab collaborations are not allowed unless stated otherwise.
- **NOT ALLOWED: not permissible collaboration or copying from colleagues or internet sources → Any detected similarity is a violation of academic code → code committee.**
- **Distractions (e.g., laptops, tablets) are not allowed during lecture except with permission.**

Lab TA: Chhay Tann





Examples of allowed & not-allowed lab discussions

- Allowed discussions should be centered on essential or common factor lab issues. Examples:
  - Where is that menu option to determine the pin locations?
  - Do you know what does this error message mean?
  - Do you remember the name for command that does …?
  - How can I prepare my project archive?

- Discussions on lab design **choices** are NOT allowed:
  - Did you design a 2-stage or 3-stage pipeline?
  - How did you manage to get your design so fast?
  - How many elements of the internal memory did you use?