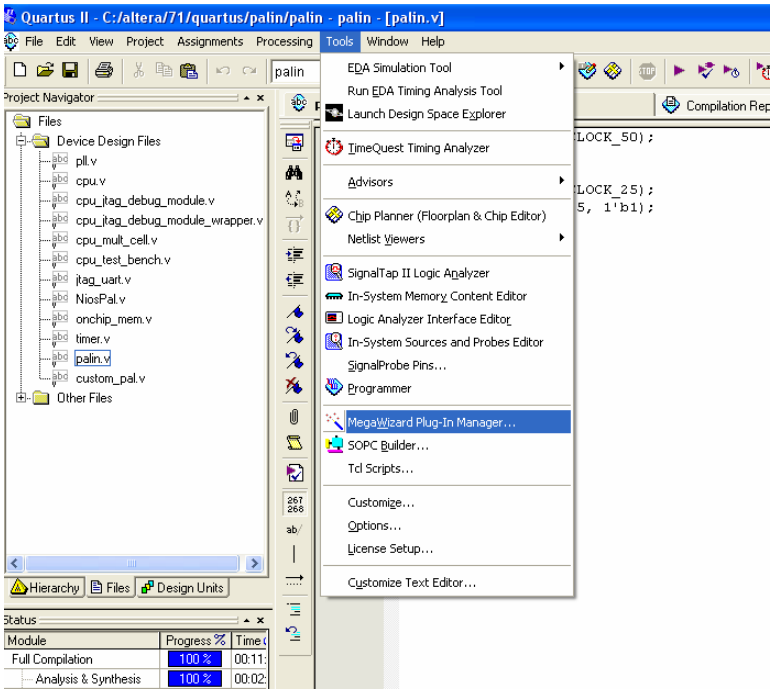
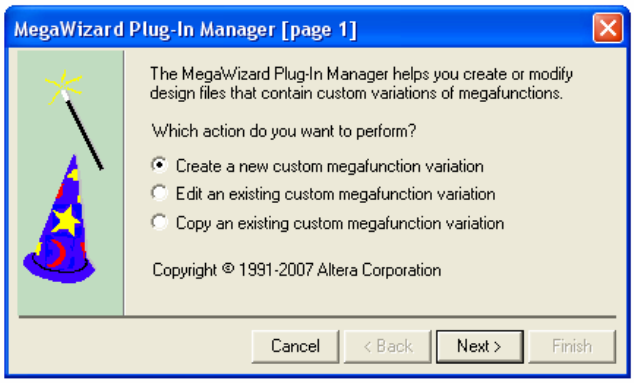
Tutorial: Adjusting the frequency of your Nios II system using PLLs (Phase Locked Loop) plug-ins

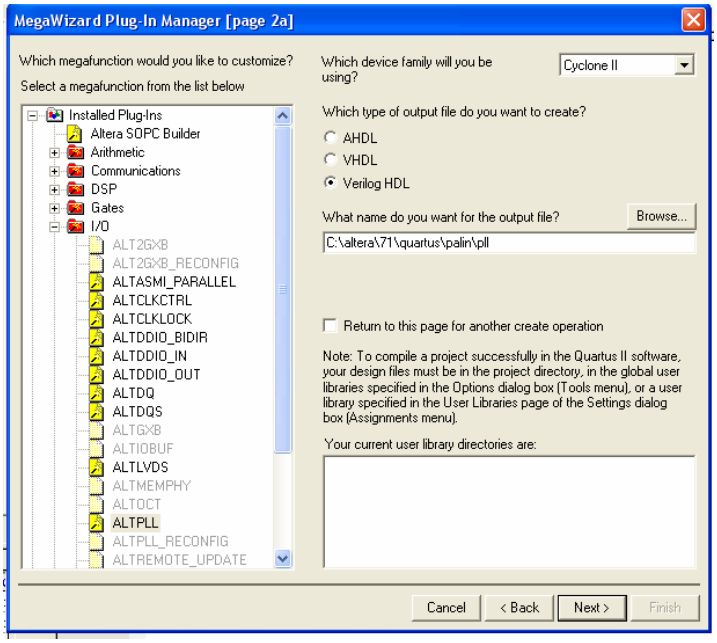
- From the Tools menu, choose MegaWized Plug-In Manager



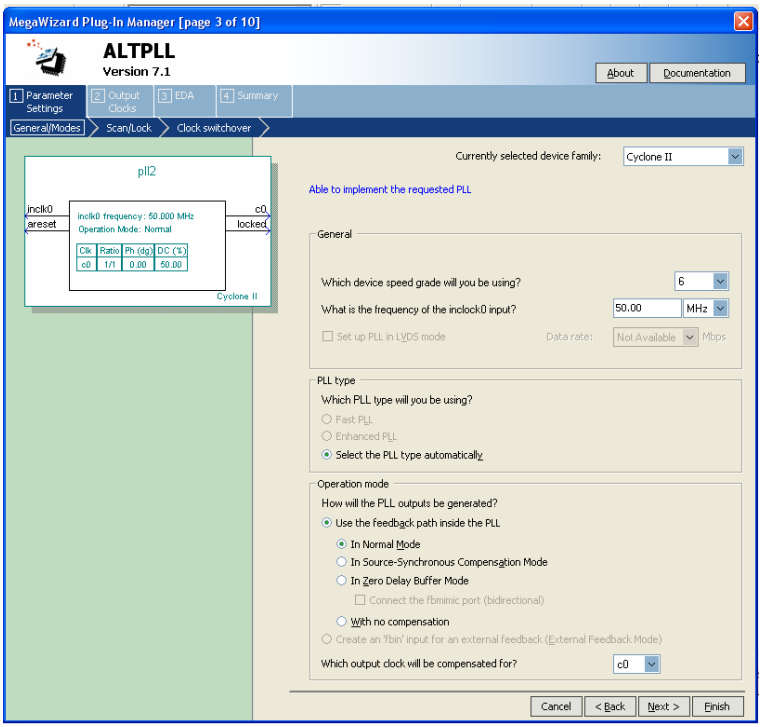
- Choose Create a new custom megafunction variation. Note that if you already have an PLL instance then you need to modify its frequency then choose the second option “Edit…” and then load the file of your existing PLL.



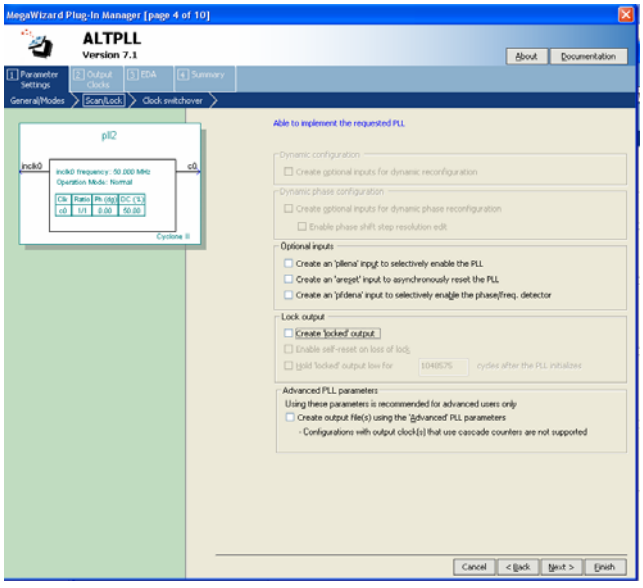
- Choose the type of your component ALT_PLL from the I/O section and name it, say “pll”



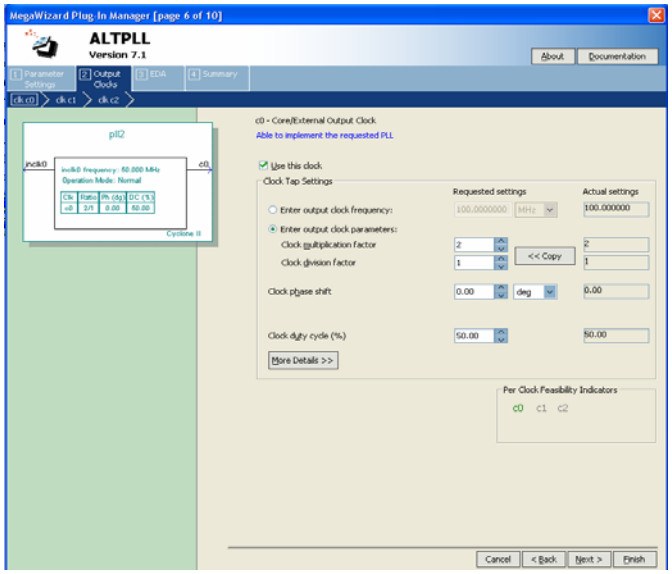
- Then change the input frequency to 50MHz



- Uncheck the ‘areset’ input (we do not need to reset the PLL) and the locked output. We want the PLL simple.



- Press the next step and then another next then adjust the output frequency by changing the divisor and the multiplier



- Then finalize the design and include the resultant file in your project. You would need to instantiate an instance of the module “pll” in your design. For example, you can have pll pll1(CLOCK_50, CLOCK_100); where CLOCK_100 is a wire than is the clock input to your Nios II system (see the Nios II tutorial).