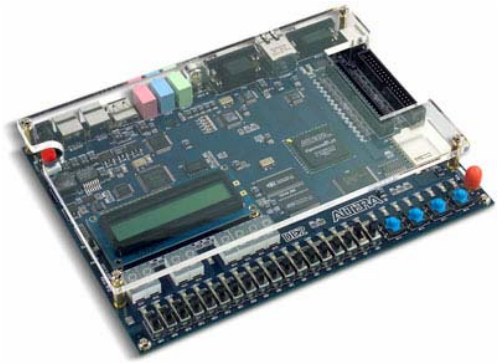
New Class Fall'07
ENGN2911X. Reconfigurable Computing

Driven by recent innovations in Field-Programmable Gate Arrays (FPGAs), reconfigurable computing offers unique ways to accelerate key algorithms. FPGAs offer a programmable logic fabric that provides the necessary hardware and communication assets to develop rapid hardware prototypes and to exploit parallelism opportunities arising in various algorithms. By mapping algorithms directly into programmable logic, FPGA accelerators can deliver 10X-100X performance increases over generic processors for a large range of application domains.

The class will cover the following topics:

- Programmable logic technology overview.
- Fundamentals of reconfigurable computing.
- Hardware programming languages (Verilog).
- High-level synthesis languages (SystemC).
- FPGA communication architectures.
- Soft multi-core processing environments.
- Acceleration of key algorithms in various scientific fields (e.g. signal and image processing, bioinformatics and robotics).
- Rapid prototyping skills with Altera's DE2 board.
- The class will include hands-on projects.



Instructor: Prof. Sherief Reda (sherief_reda@brown.edu).
Meeting Times: T. and Th. 2:30-3:50 PM.
Location: TBD.
First class meeting: Sept 11th 07.