EN2911X: Reconfigurable Computing
Lecture 02: Programmable Logic Technology (1)

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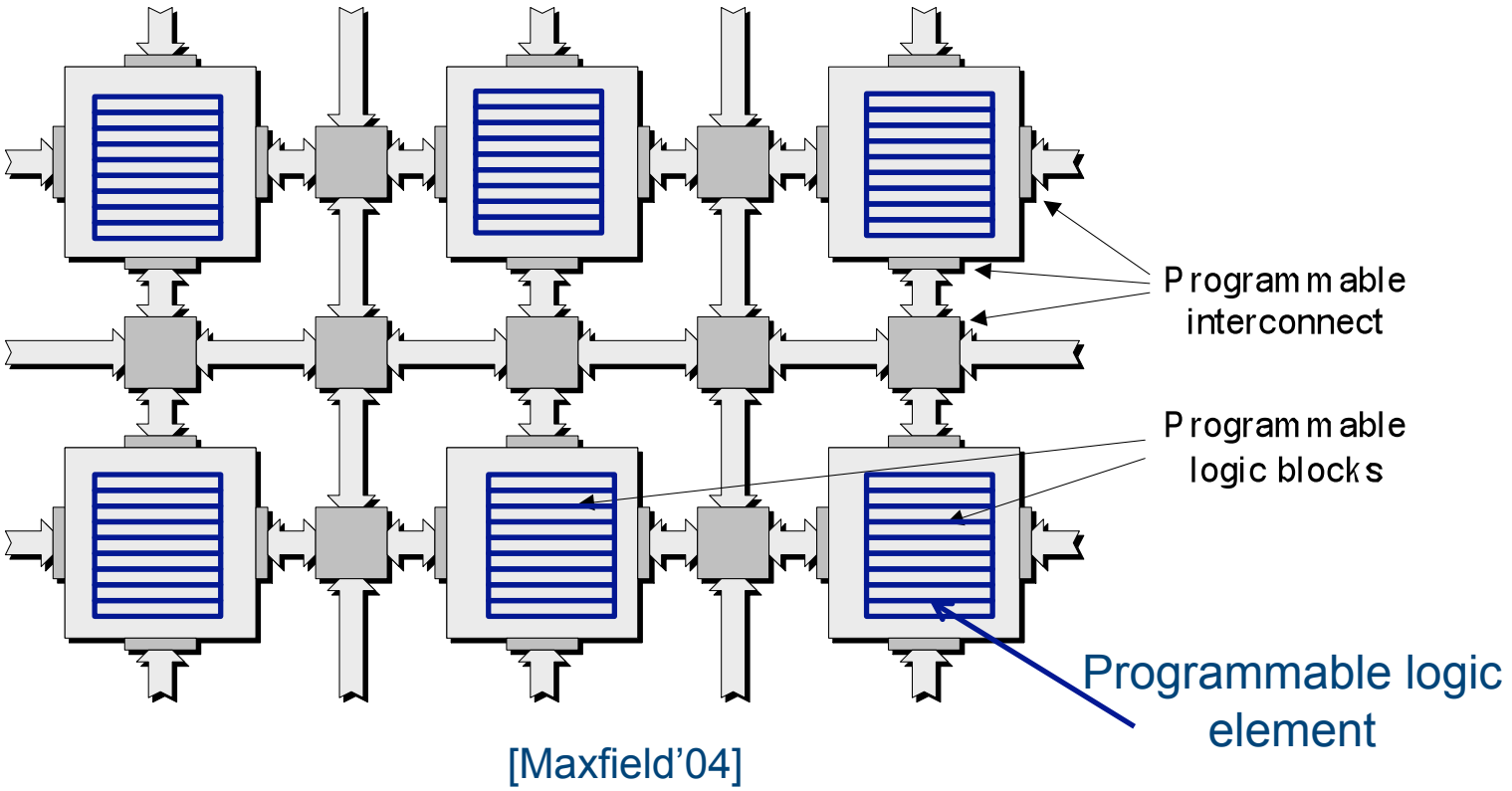
Fall '09

FPGA architecture



[Maxfield'04]

Objective of this lecture: study organization of programmable logic blocks and interconnects

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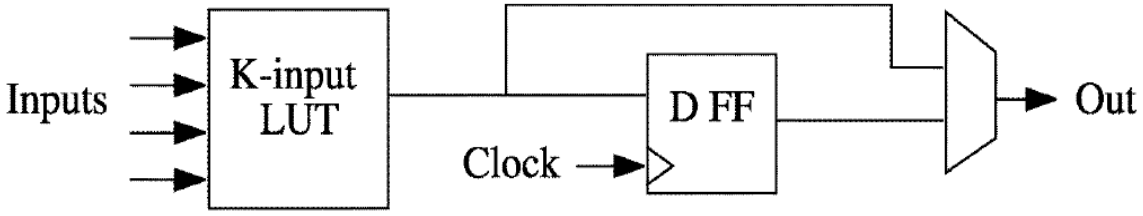
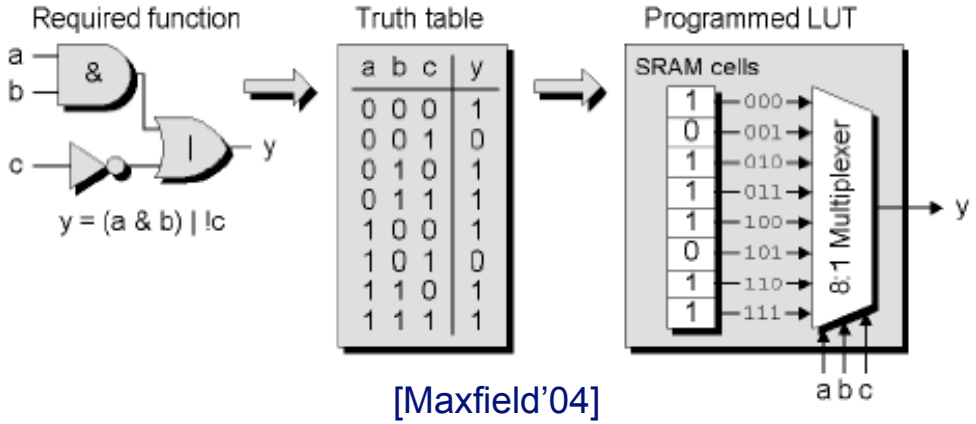
Block logic element



[Rose'04]



[Maxfield'04]

- How is the number of bits in a K-input table?
- How many Boolean functions can a K-input LUT implement?
- What is the best LUT size?

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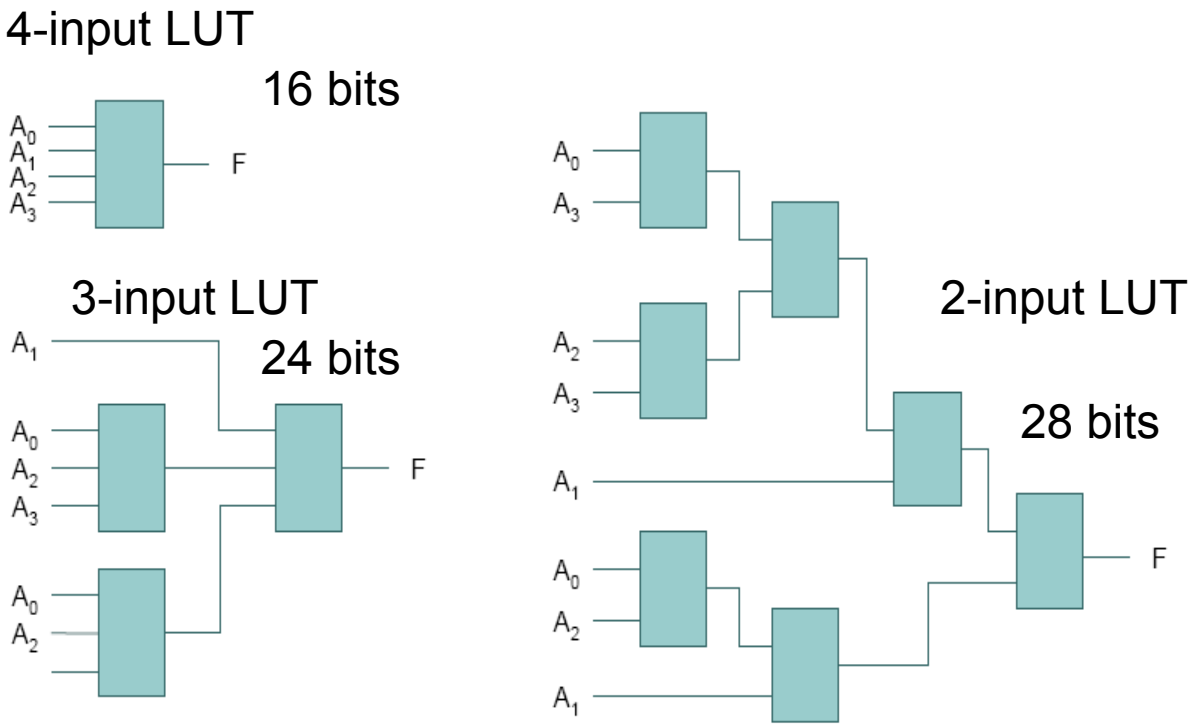
Example

[from J. Zambreno]

$$F = A_0A_1A_3 + A_1A_2\bar{A}_3 + \bar{A}_0\,\bar{A}_1\,\bar{A}_2$$



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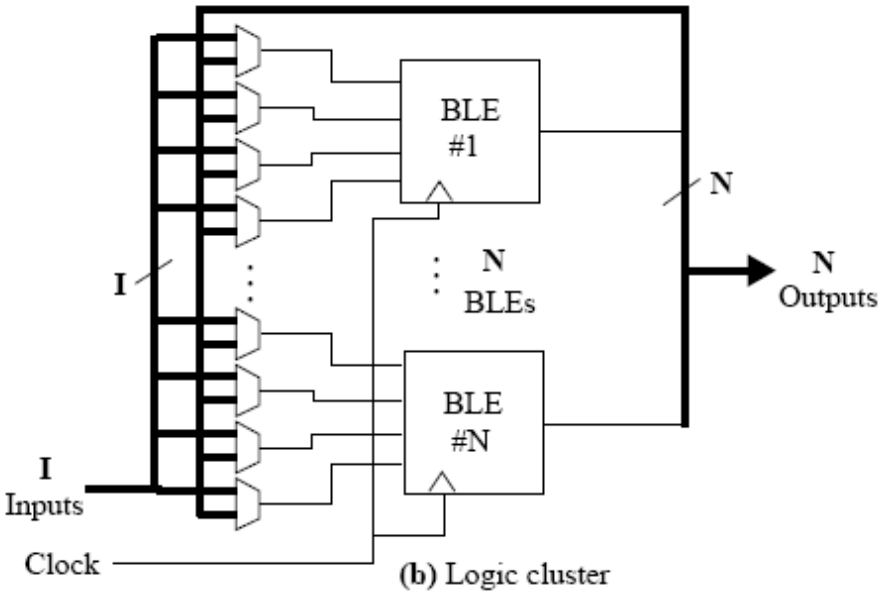
Logic block clusters (logic array block LAB, configurable logic block CLB)

- Assume K-input LUT in each BLE and assume N BLEs per logic cluster
- The BLEs in each logic clusters are *fully connected* or "nearly-fully" connected
- What are the best values for I, K, and N?



[Betz-Rose 97]

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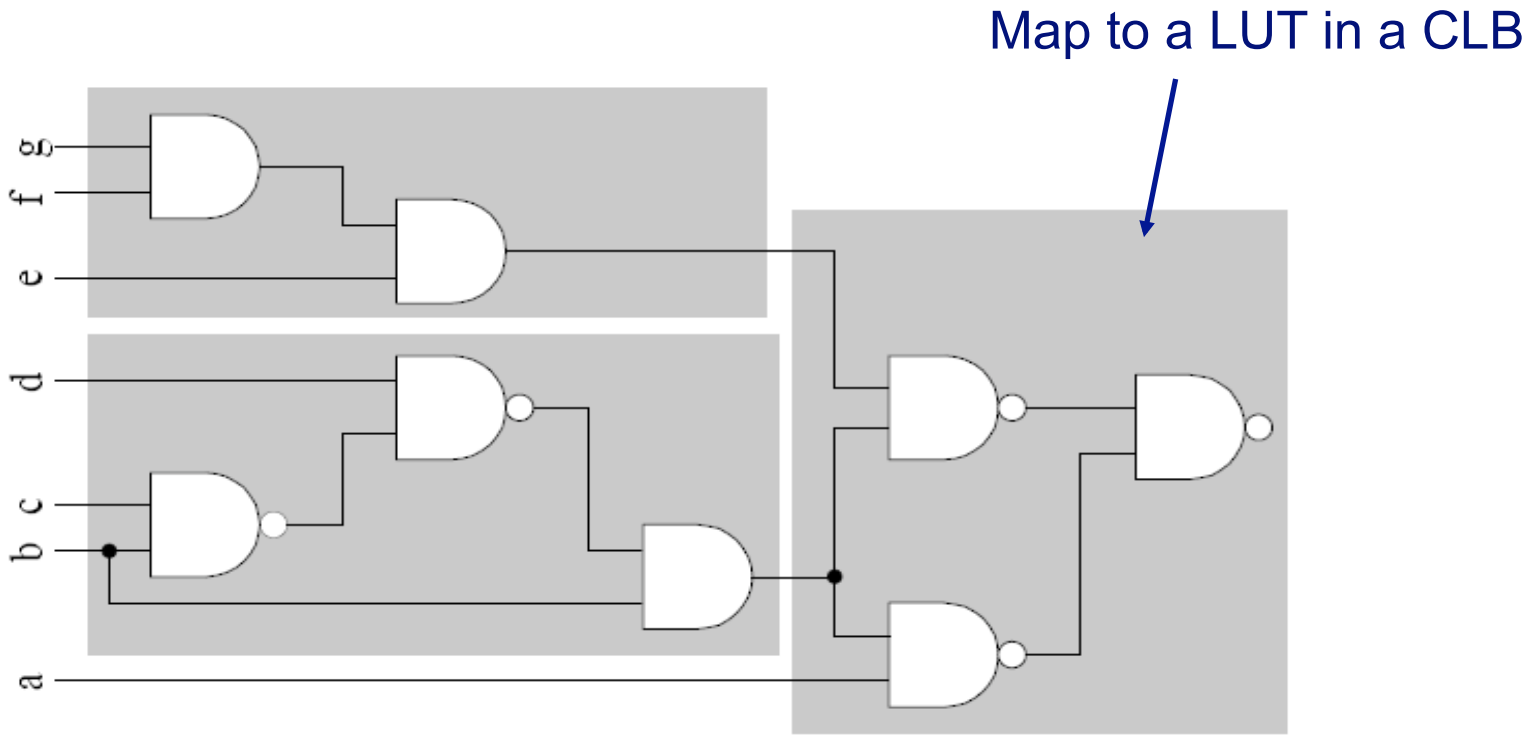
To implement in FPGAs, designs need to be decomposed and mapped to LBs



[Figure form Cong FPGA'01]

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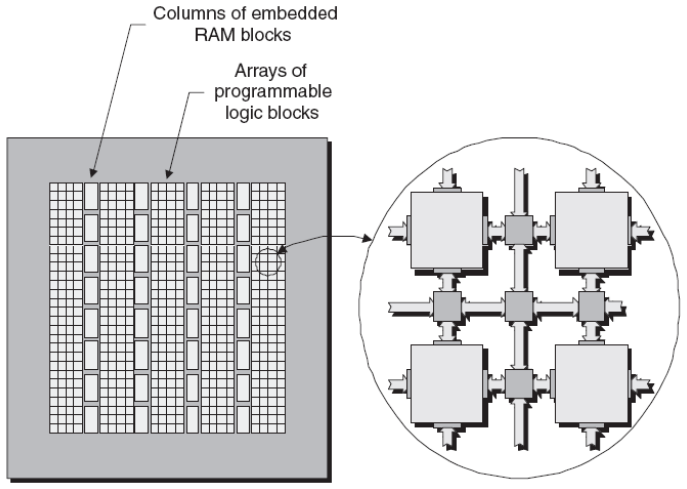
Heterogeneous reconfigurable logic

- Reconfigurable fabric might contain non-reconfigurable elements that interface to the logic blocks through the programmable interconnect fabric
- Examples:
  - Embedded memory
  - Embedded multipliers, adders, MAC
  - Embedded processors

Embedded memory blocks

- Costly to implement memory with configurable logic blocks → add hard chunks of RAM blocks
- Position/size vary depending on the FPGA device. Size varies from few thousands (or tens of thousands) per RAM block
- Each block can be used independently or combined to form larger RAM blocks
- Could be single or dual-port RAMs



[Maxfield'04]

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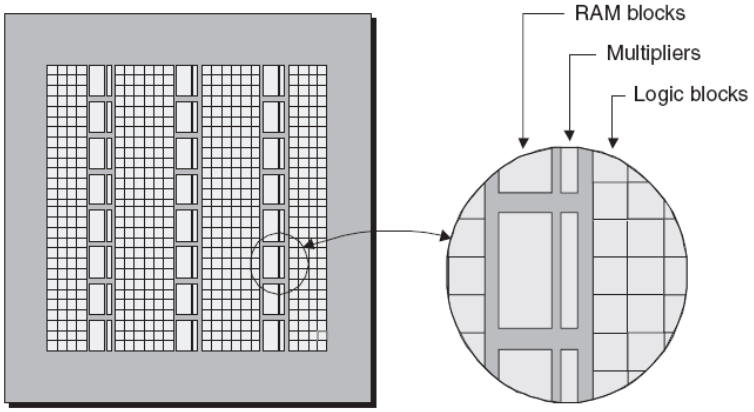
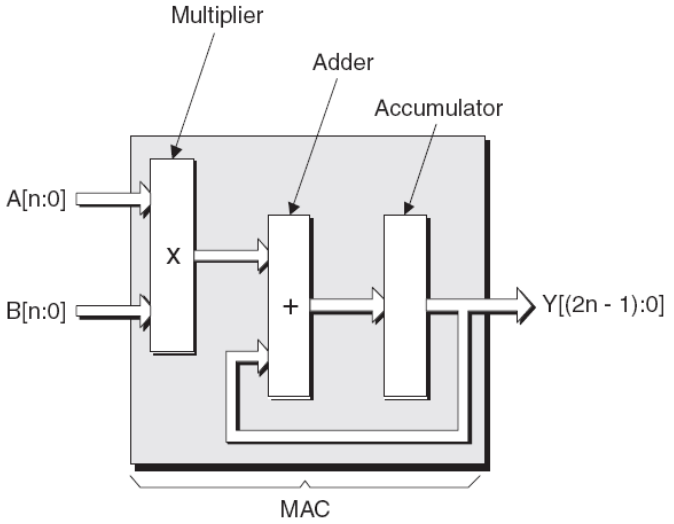
Embedded multipliers and adders

- Multipliers are inherently slow if implemented by connecting a large number of programmable logic blocks → add hard-wired multiplier blocks
- Typically located close to the embedded RAM blocks
- Some FPGA use Multiply-And-Accumulate (MAC) blocks (useful in DSP applications)





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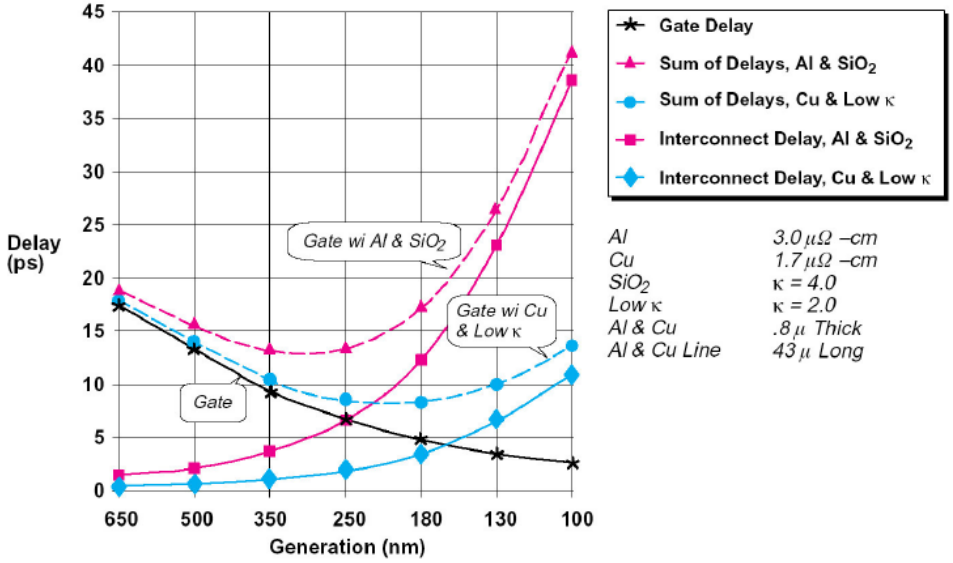
Programmable routing

- Wires provide the necessary communication fabric to route the output of one computational node to the inputs of another computational node
- Why routing is very crucial?
  - Routing resources occupy a larger area than logic resources in an FPGA
  - Wire delay grows quadratically as a function of its length
  - Technology scaling reduces device delay but increases wire delay



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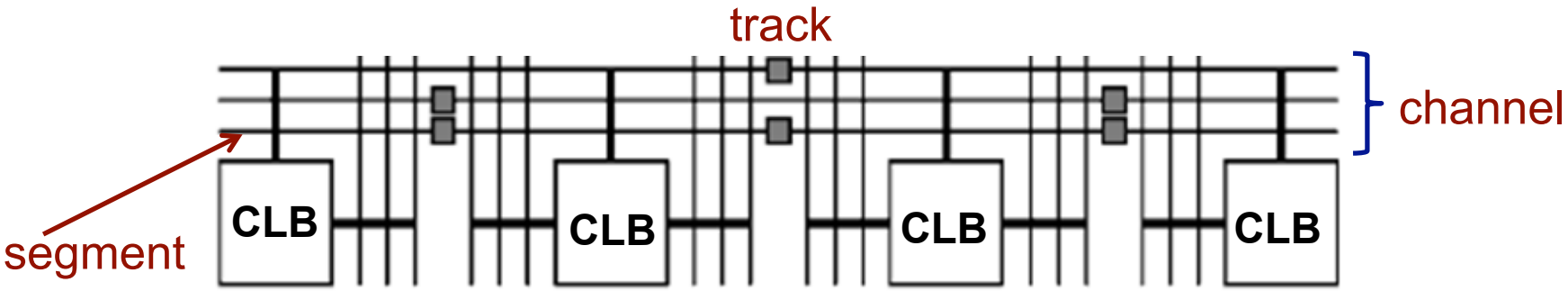
General routing definitions



- A *wire segment is a wire unbroken by* programmable switches
- A *track is a sequence of one or more wire* segments in a line. The segments could be connected by switches at their ends
- A *routing channel* is a group of parallel tracks. The channel *width* is the number of tracks in the channel

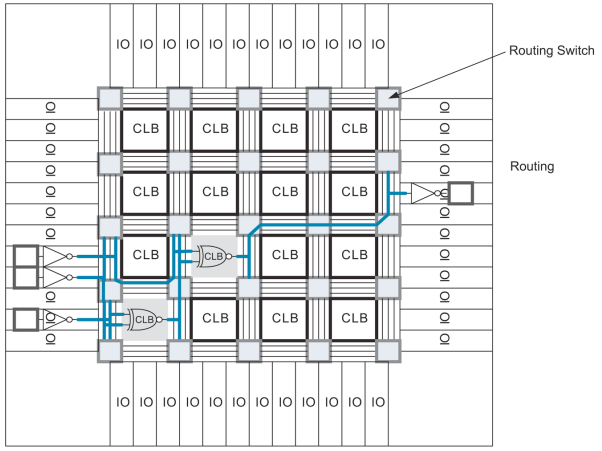


FIG 8.24 Personalized and routed FPGA

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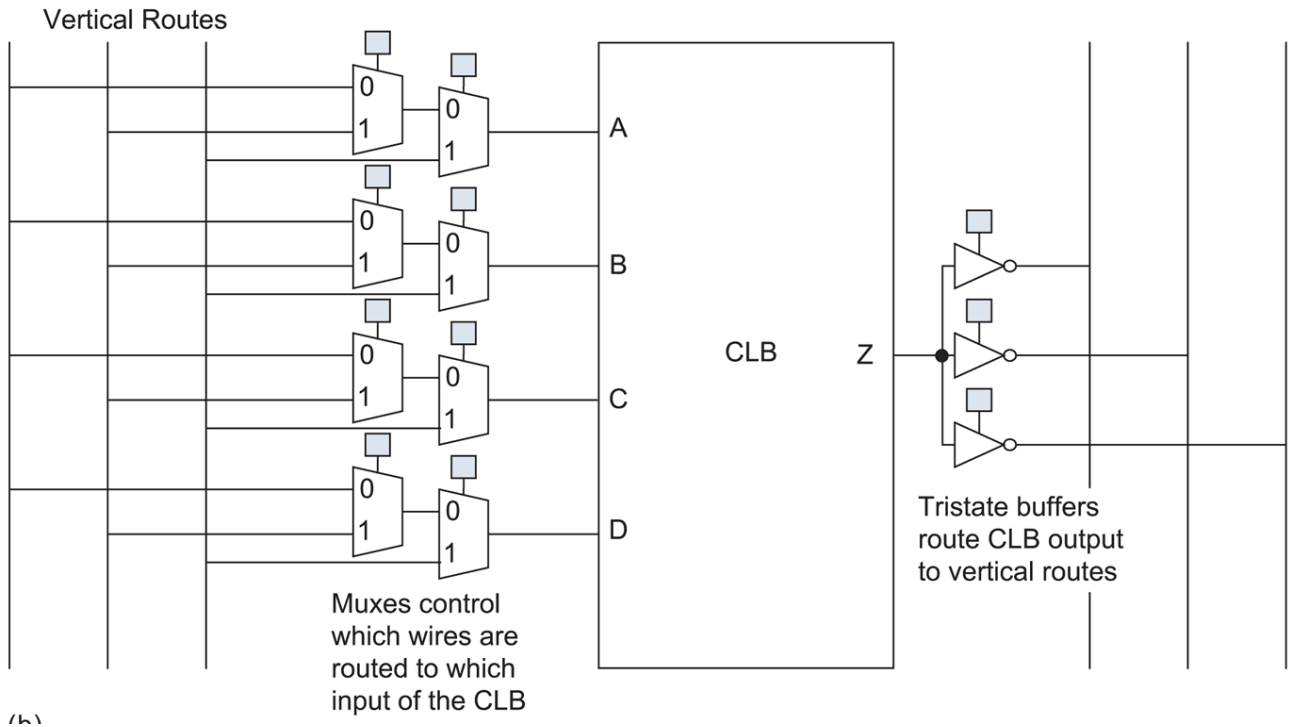
Connection blocks: formed where CLB input or output pins connect to the routing channels



Life would have been easy if only logic blocks within the same column or row need to communicate!

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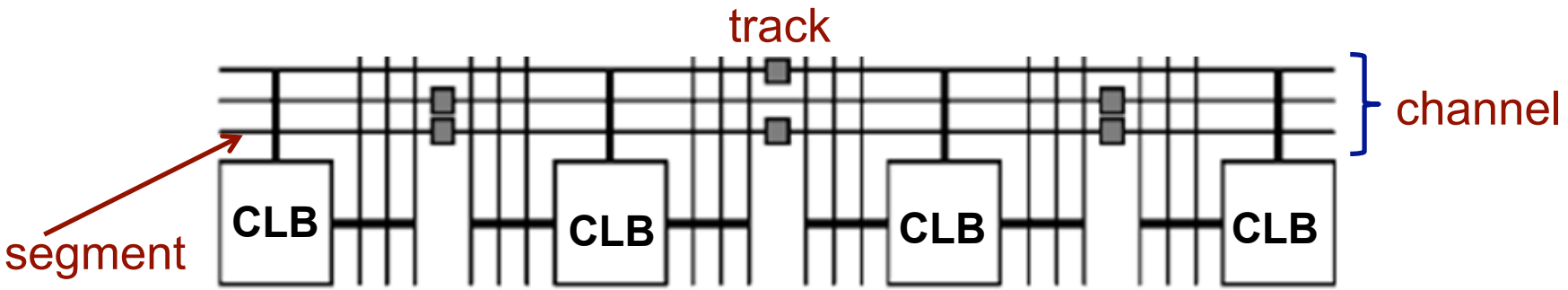
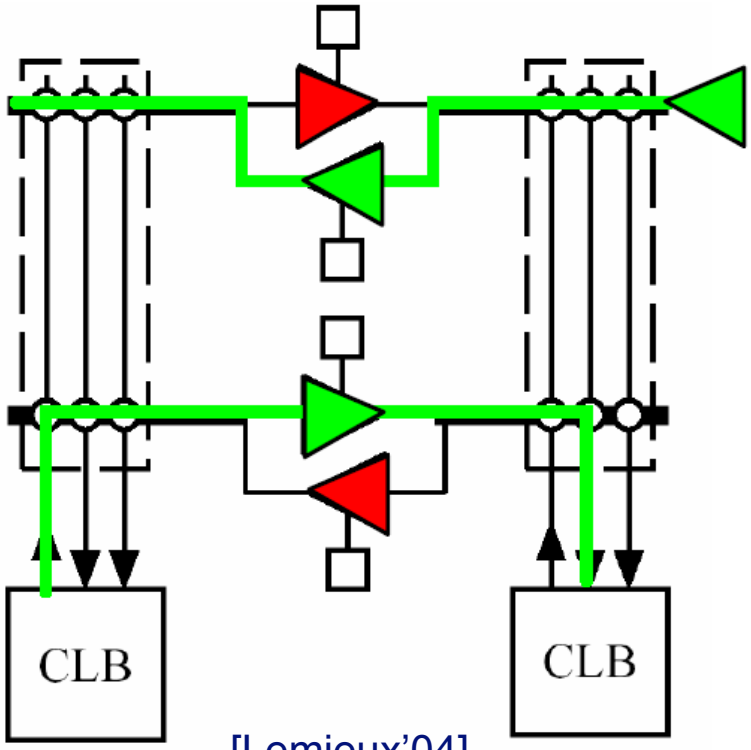
Segment-segment switch design for bidirectional wires





[Lemieux'04]

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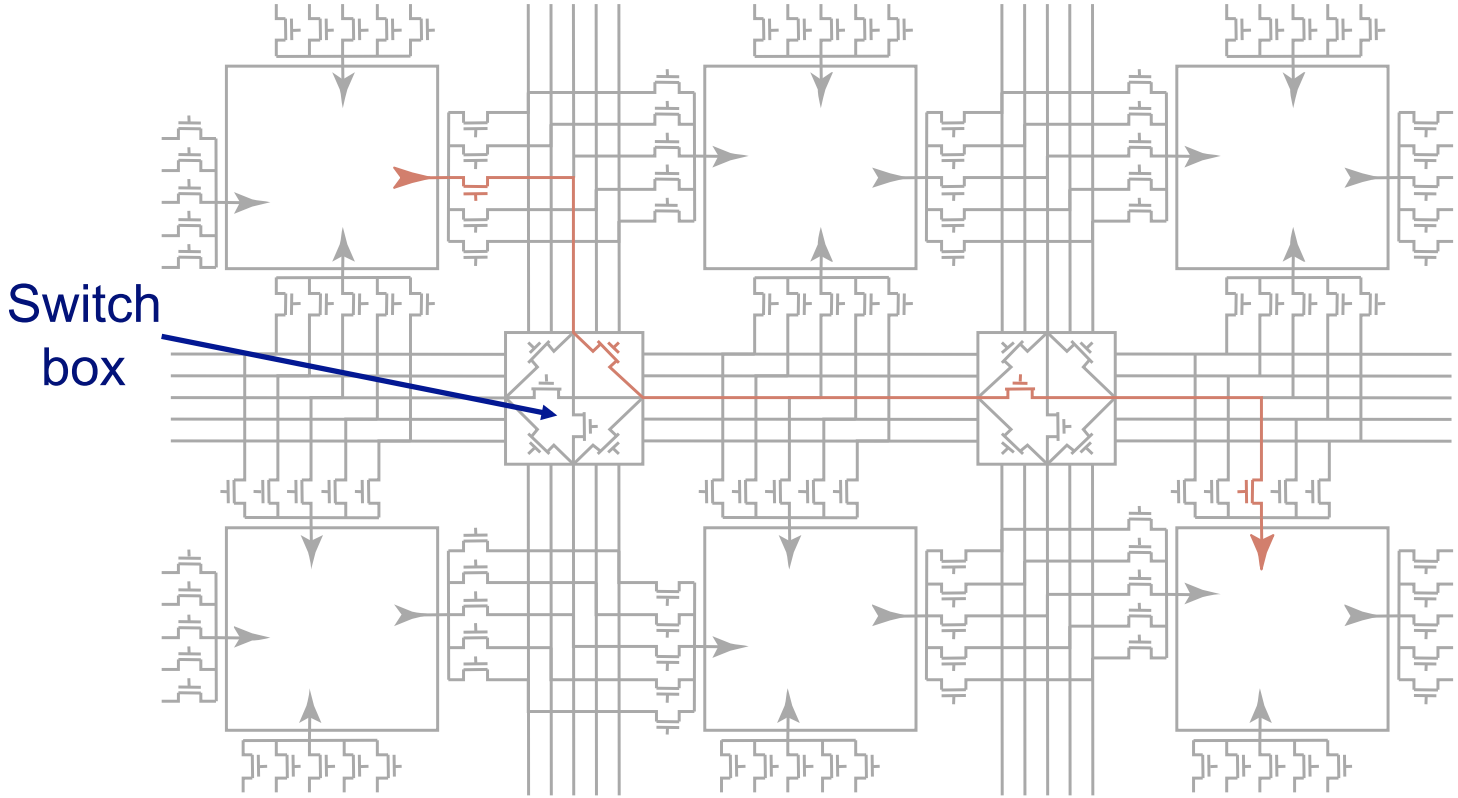
Switch blocks: formed wherever horizontal and vertical channels intersect



Switch box size grows quadratically as a function of the number of its input wires

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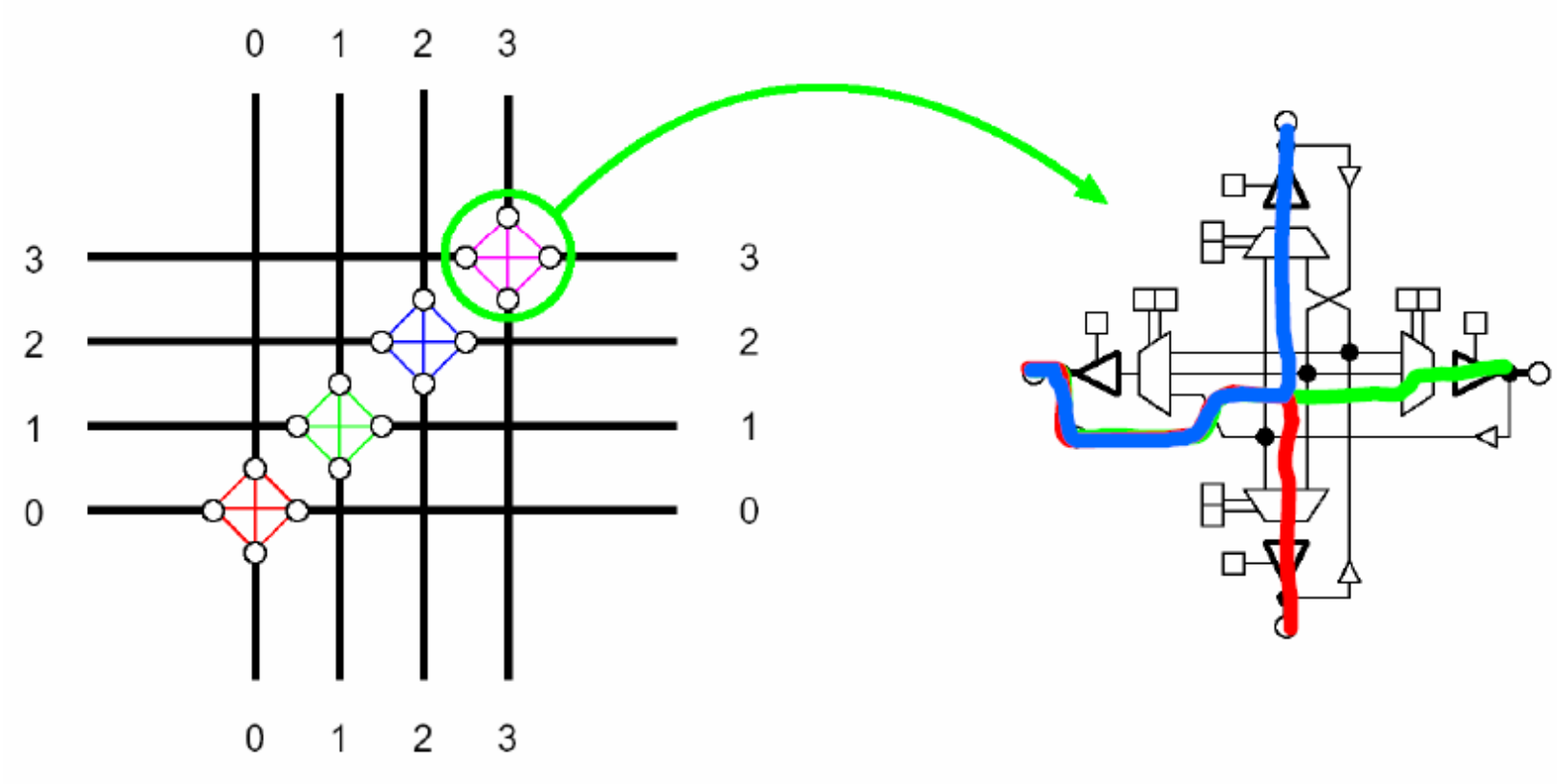
Bidirectional switch details



[Lemieux'04, Tessier]

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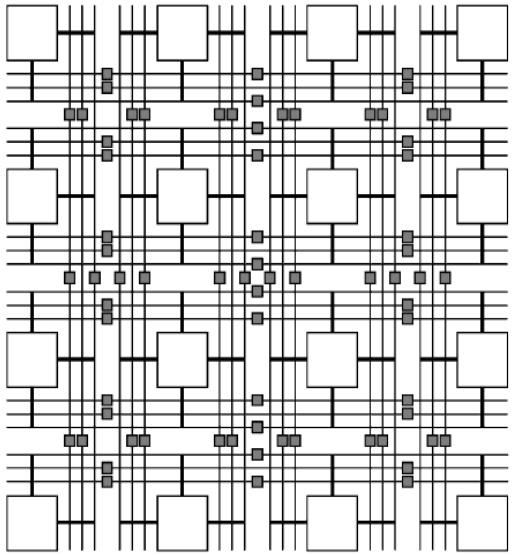
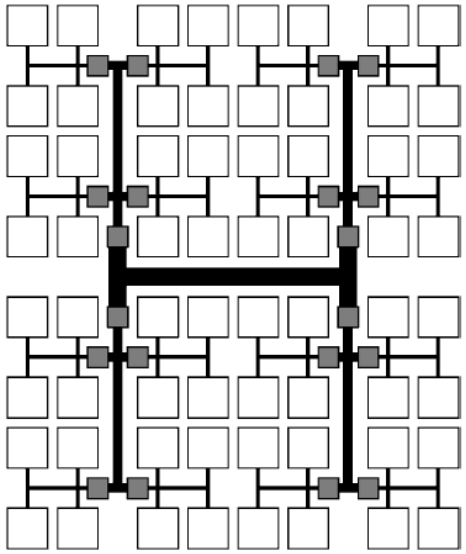
Segmented and hierarchical routing

segmented routing



- Short wires accommodate local traffic
- Short wires can be connected together using switch boxes to emulate longer wires
- Also contain long wires to allow efficient communication without passing through switches

hierarchical routing



- Routing within a “group” of logic blocks occur at the local level
- Longer hierarchical wires connect different groups

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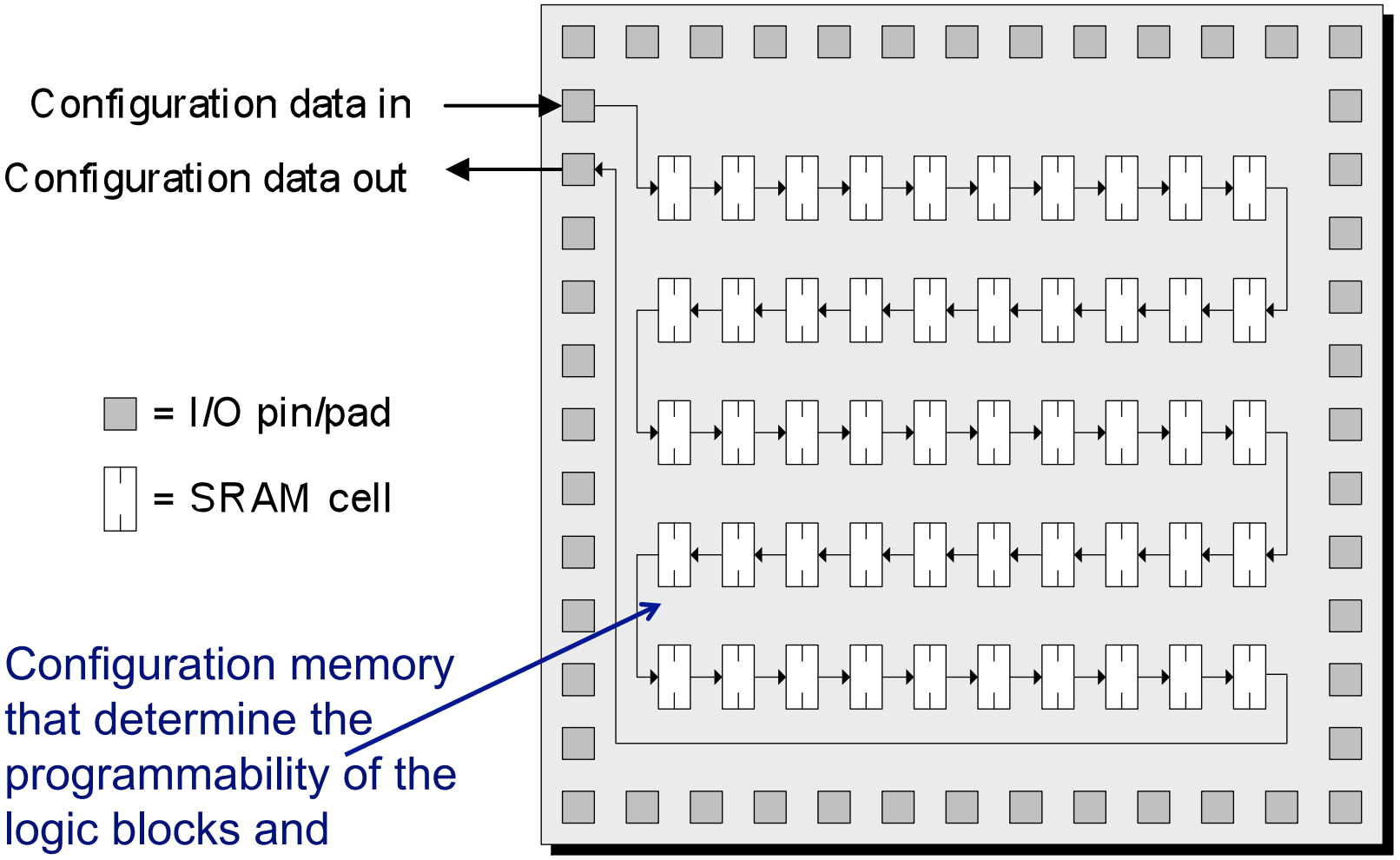
Programming the FPGA



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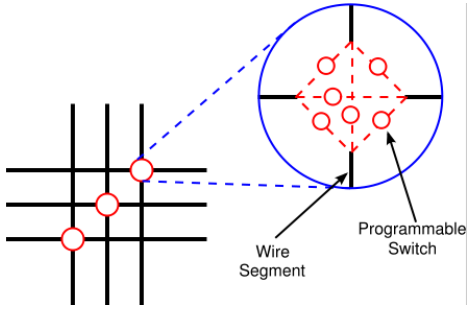
Programmable switch technology

Anti-fuse

Switch by default is OFF; when programmed it is ON.

Advantages:
- negligible delay
- small area overhead

Disadvantages:
- not really reconfigurable; one time programmable



Flash

Switch by default is ON; when programmed it is OFF.

Advantages:
- programming not lost when device is turned off.

Disadvantages:
- requires more manufacturing steps

SRAM

SRAM bit cell stores the programmability of the device

Advantages:
- can be reconfigured quickly and as repeatedly as required
- no special fabrication steps

Disadvantages:
- takes more area
- loses charge when turned off

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Assigned readings

- For Thursday Sept 17: Reconfigurable computing: A survey of systems and software. K. Compton & S. Huack (Sections 1-3)
- You have to submit a 1 (or more) page summary of the paper (main ideas + critique) before noon of the lecture day. Only use the submission form on the class website. Any summaries submitted after that time will not be looked at!