EN2911X: Reconfigurable Computing
Lecture 03: Programmable Logic Technology (2)

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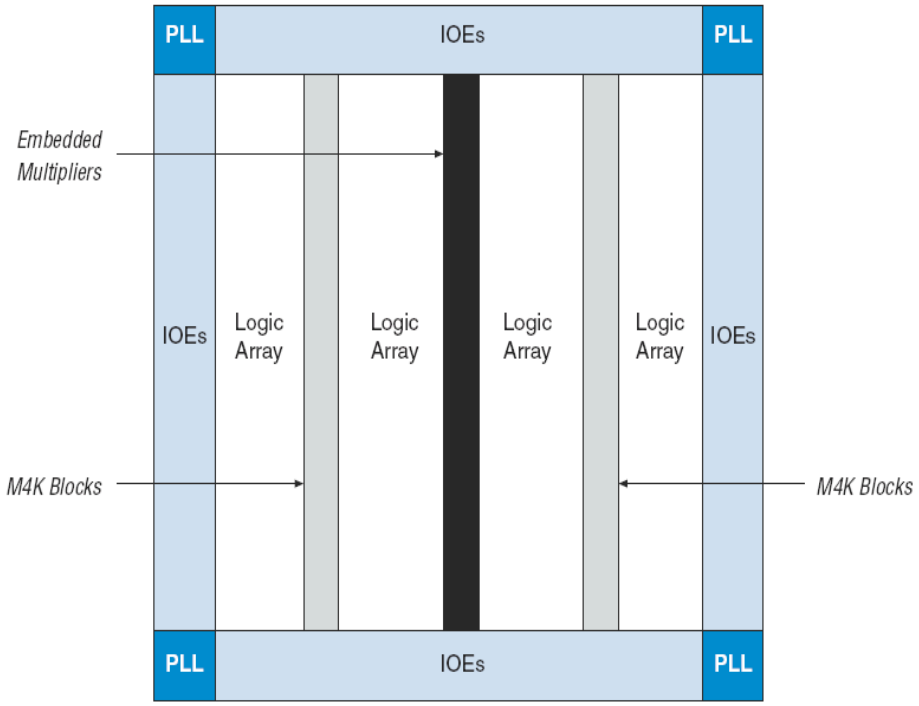
Case study: Altera's Cyclone II device



- Two dimensional array of Logic Array Blocks (LABs), with 16 Logic Elements (LEs) in each LAB.
- Embedded memory blocks (M4K) and multipliers (18x18)
- PLL (Phased Locked Loops) are used to generate clock signal for a range of frequencies
- EP2C35 (in DE2 board) has 60 columns and 45 rows for a total of 33216 LEs. 105 M4K blocks and 35 embedded multipliers.

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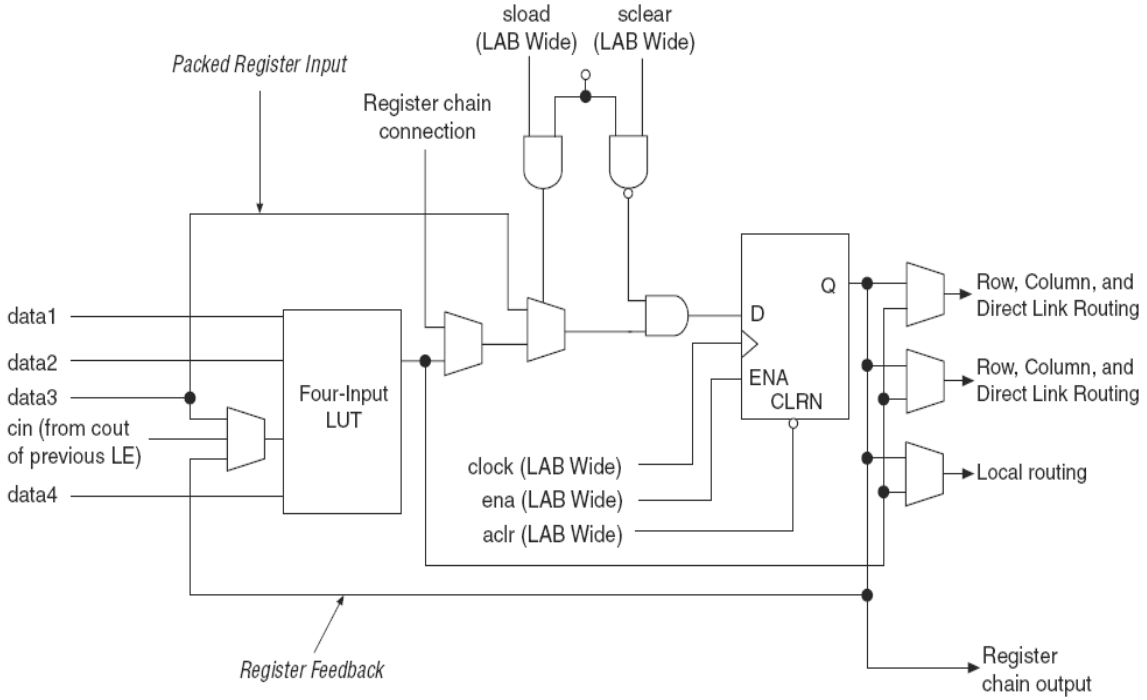
Logic element organization (normal mode)



The LE has two operating modes: normal and arithmetic

Normal mode is suitable for general logic implementation

- 4-input LUT
- 6 input connections
- 3 output connections
- LAB-wide synchronous/asynchronous clear and load signals. Clock signal

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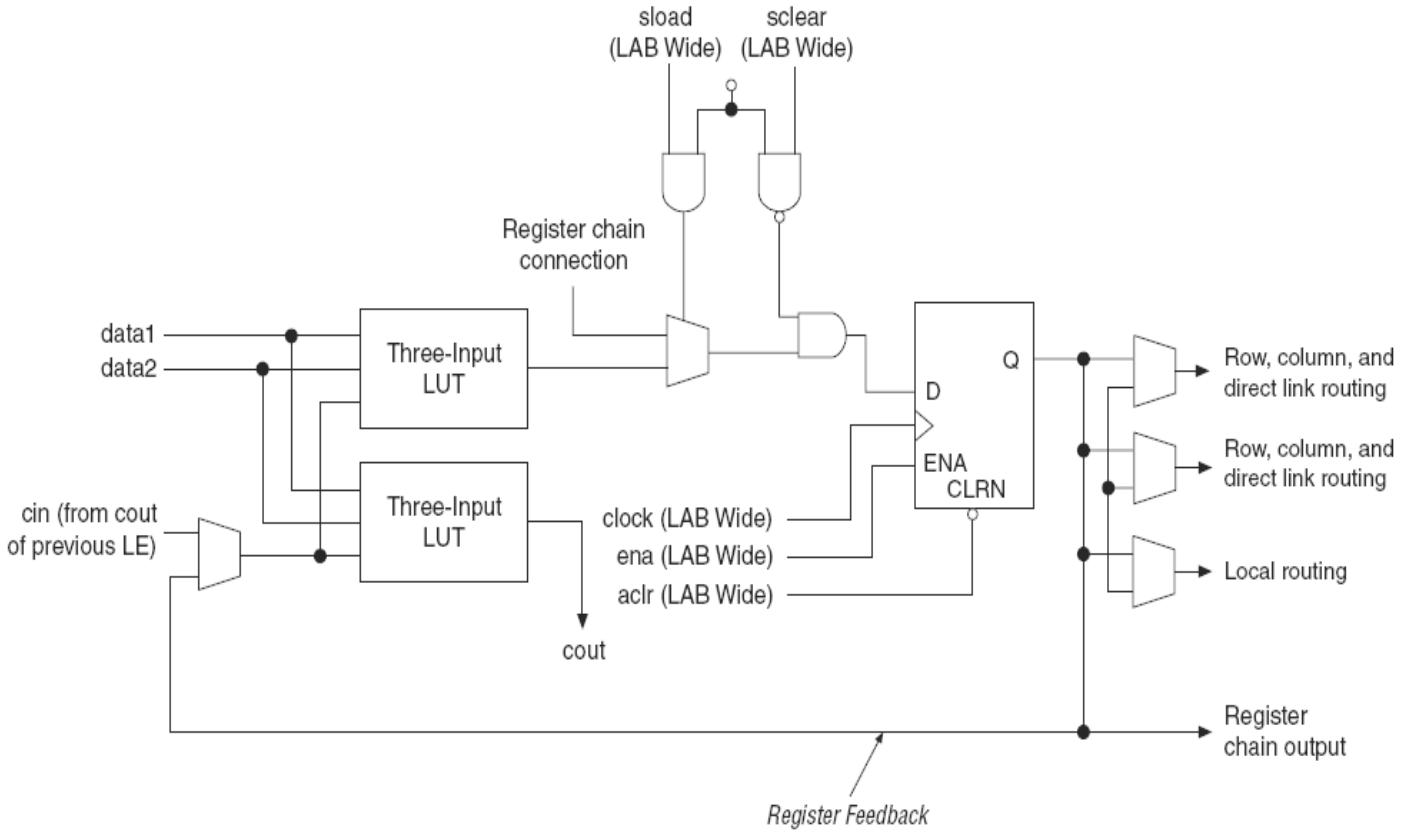
Logic element organization (arithmetic mode)



Arithmetic mode is suitable for implementing adders, counters, accumulators and comparators

- The LUT is split into two 3-input LUTs (ideal for implementing 2-bit full adders) and basic carry chain

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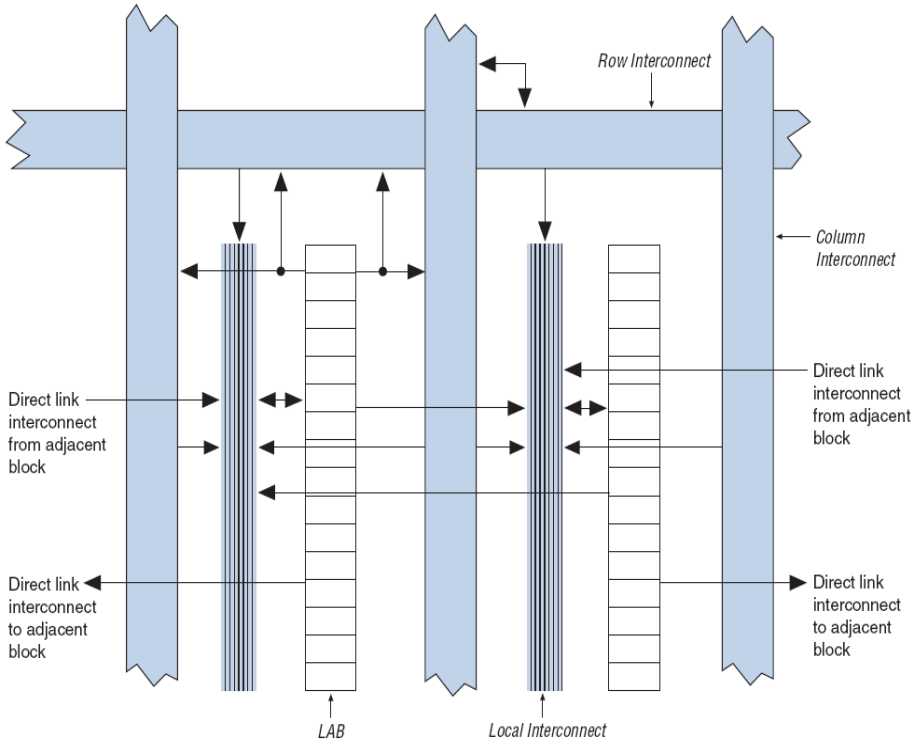
Logic array block organization



- Each LAB consists of the following: 16 LEs, LAB control signals, LE carry chains, register chains and local interconnects
- Local interconnects transfer signals between LEs in the same LAB and is driven by column and row interconnects and LE outputs within the same LAB
- Neighboring LABs, PLLs, M4K RAM and multipliers from the left and right can also drive an LAB's local interconnect
- Each LE can drive 48 Les through fast local and direct interconnects

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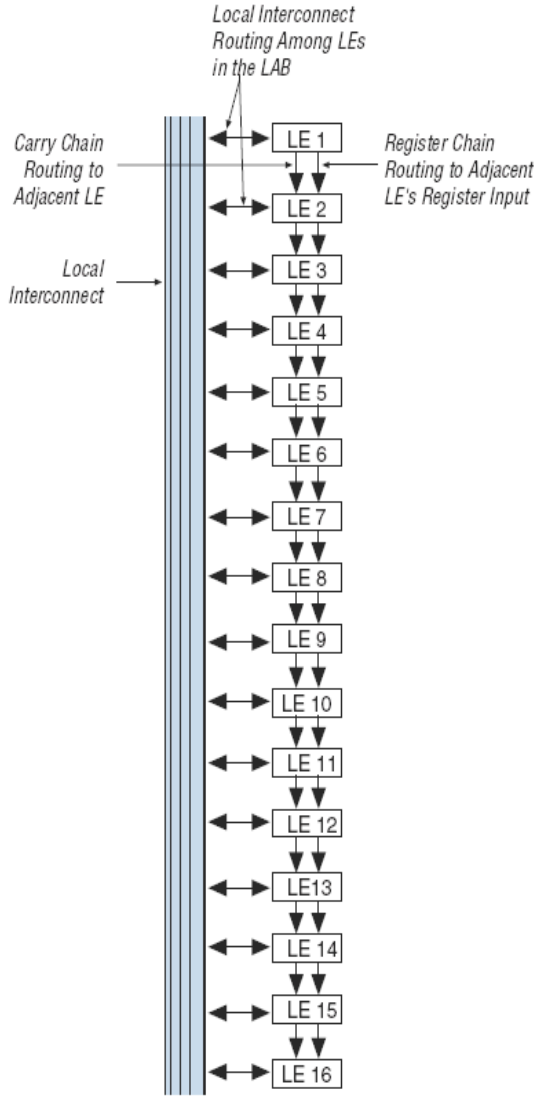
Register/carry chain connections with a LAB



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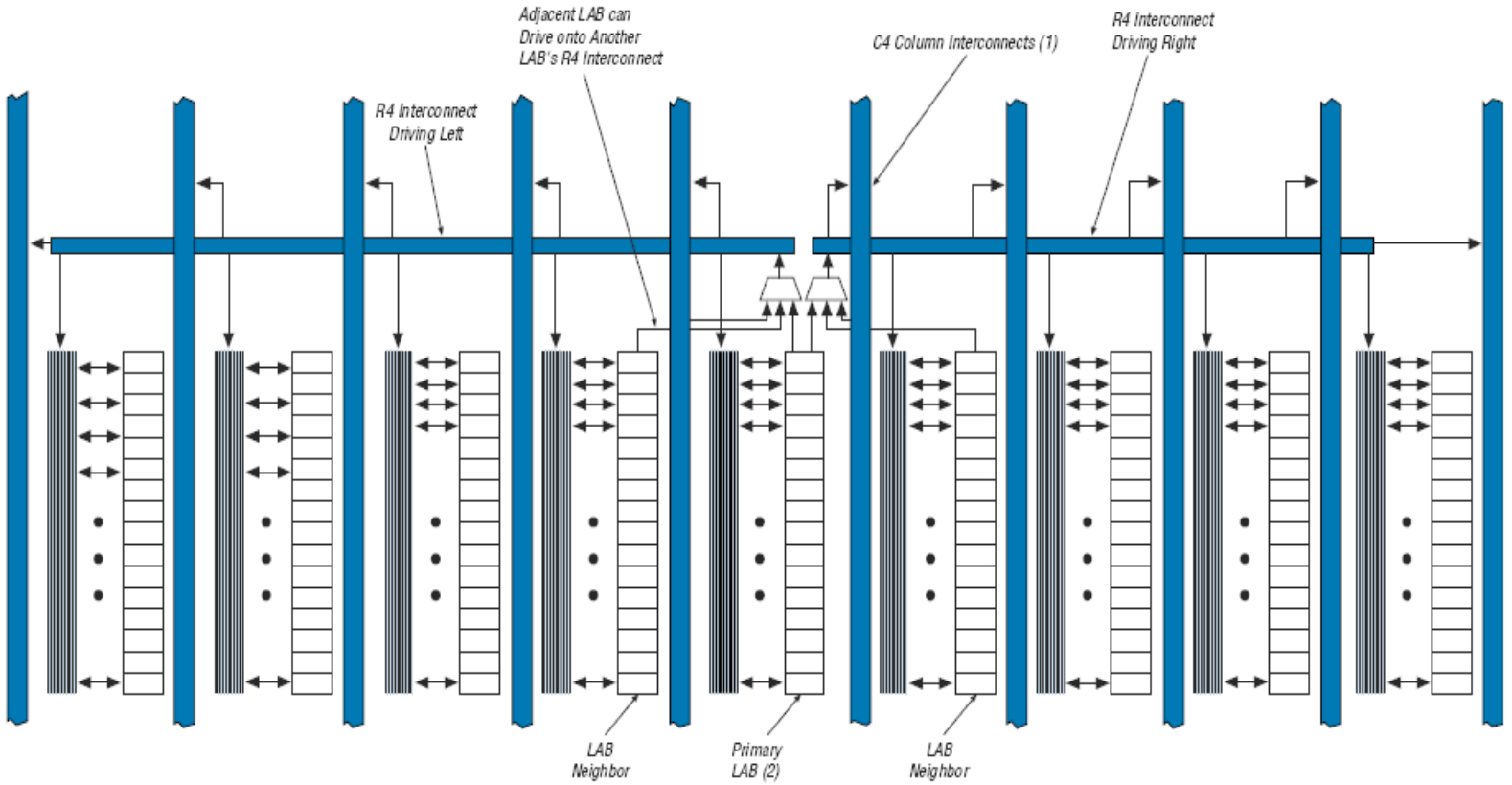
Multi-track interconnects



- Multitrack interconnect consists of row (directlink, R4, R24) and column (register chain, C4, C16)
- R4/C4 interconnects spans 4 blocks (right, left / top, down)
- R24/C16 spans 24/16 blocks and connects to R4/C4 interconnects
- R4/C4 can drive each other to extend their range

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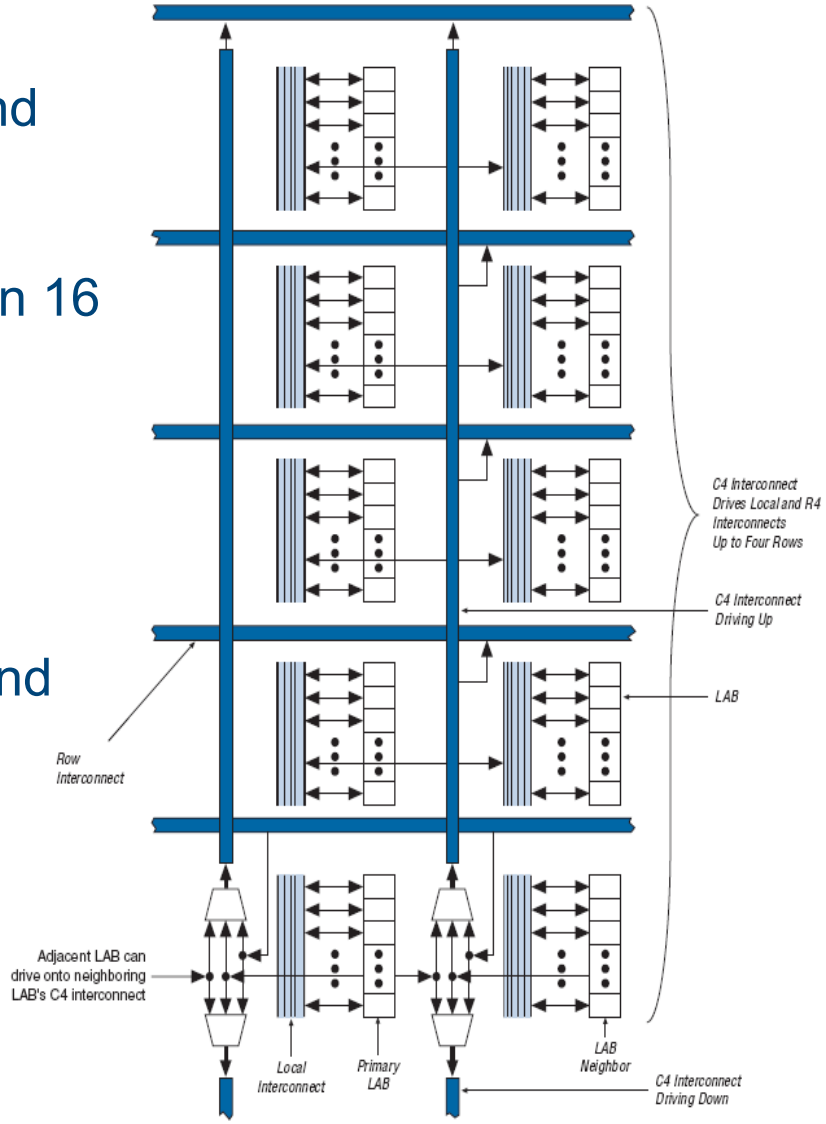
C4 interconnections

- C4 interconnects drive local and R4 interconnect up to 4 rows
- C16 column interconnects span 16 LABs and provide long column connections
- C16 column interconnects *indirectly* drive LAB local interconnects via C4 and R4 and interconnects



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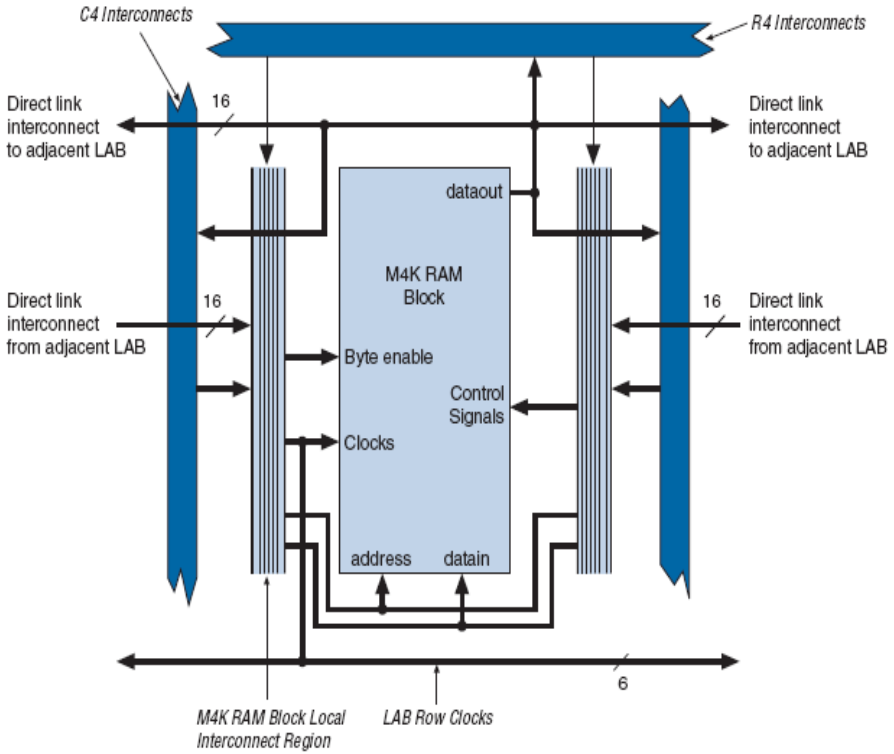
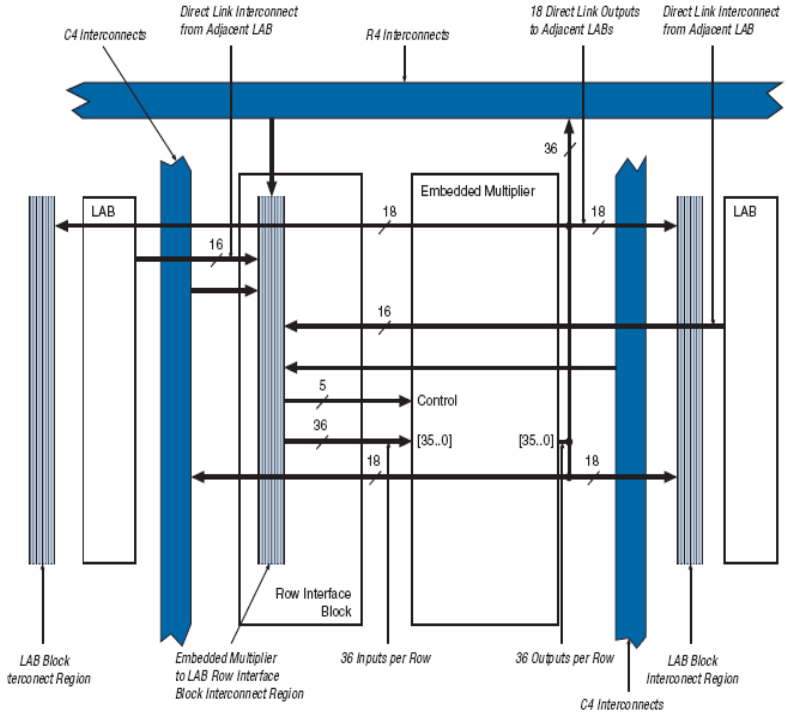
Embedded RAMs and multipliers





- 4608 RAM bits (w or w/o parity)
- 250 MHz performance
- Either single or dual port memory
- Can also be configured as FIFO

- ideal for DSP applications
- 250 Mhz performance
- Either configured as one 18 bit multiplier or two independent 9 bit multipliers

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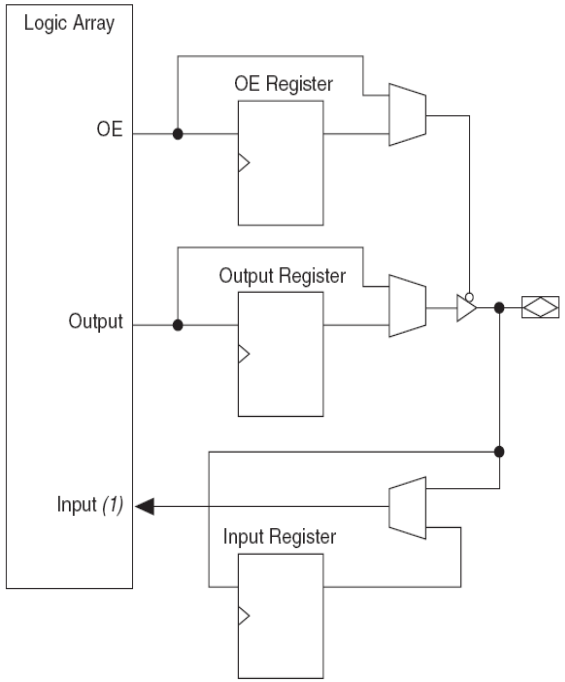
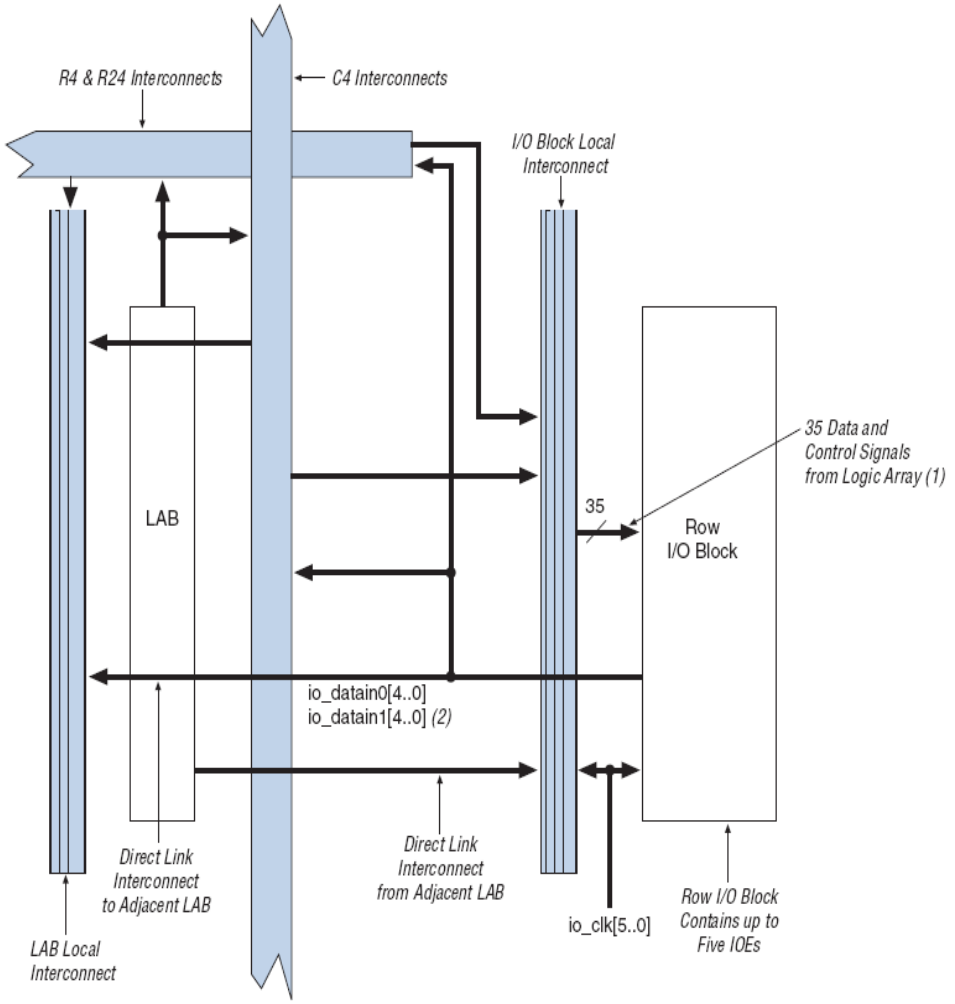
IO Element (IOE) structure





- IO Element (IOE) structure (allows bidirectional signals)
- 5 IOE per row I/O block
- Row I/O blocks drive C4, R4, R24 c direct link interconnects.
- Column I/O blocks drive C4, C16 interconnects

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