



Behavioral Modeling (Quartus II Verilog HDL Support)

Quartus II support for behavioral modeling is described below. Section numbers match those in the IEEE Std 1394-2001 *IEEE Hardware Description Language Based on the Verilog Hardware Description Language* manual.

Section	Verilog HDL Construct	Quartus II Support
9.2	Procedural Assignments	Supported as defined in subsections 9.2.1 and 9.2.2.
9.2.1	Blocking Procedural Assignments	Supported.
9.2.2	Nonblocking Procedural Assignments	Supported.
9.3	Procedural Continuous Assignments	Not supported.
9.3.1	Assign and Deassign Procedural Continuous Assignments	Not supported.
9.3.2	Force and Release Procedural Continuous Assignments	Not supported.
9.4	Null Statements	Supported for all statements except For Statements.
9.4	Conditional Statements(If-Else Statements)	Supported.
9.5	Case Statements	Supported.
9.6	Looping Statements	Supported.
9.7	Procedural Timing Controls	Supported as defined in subsections 9.7.1 through 9.7.6.
9.7.1	Delay Controls	Ignored for synthesis.
9.7.2	Event Controls	Supported at the top of Always Constructs only.

9.7.3	Named Events	Not supported.
9.7.4	Event or Operators	Supported.
9.7.5	Level-Sensitive Event Controls (Wait Statements)	Not supported.
9.7.6	Intra-Assignment Timing Controls	Ignored for synthesis.
9.8	Block Statements	Supported as defined in subsections 9.8.1 and 9.8.2.
9.8.1	Sequential Blocks (Begin-End Blocks)	Supported.
9.8.2	Parallel Blocks (Fork-Join Blocks)	Not supported.
9.9	Behavioral Constructs	Supported as defined in subsections 9.9.1 and 9.9.2.
9.9.1	Initial Constructs	Supported for specifying power-up conditions.
9.9.2	Always Constructs	Supported.



Note: Support for each Verilog HDL construct is described with one of the following terms:

- **Supported**—The Quartus II software offers full support for the construct.
- **Not-supported**—The construct cannot be used in a [Verilog Design File \(.v\)](#). If used, the construct causes an error when the Quartus II software compiles the file.

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