Brown University
Division of Engineering
EN2911X Reconfigurable Computing.
Prof. Sherief Reda
HW/LAB 01 (50 points). Due Date: Friday, Sept 19th 2014.

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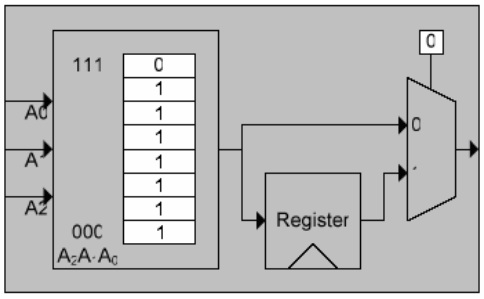
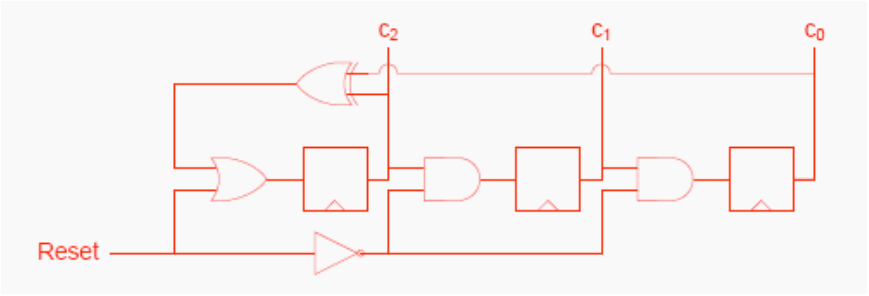
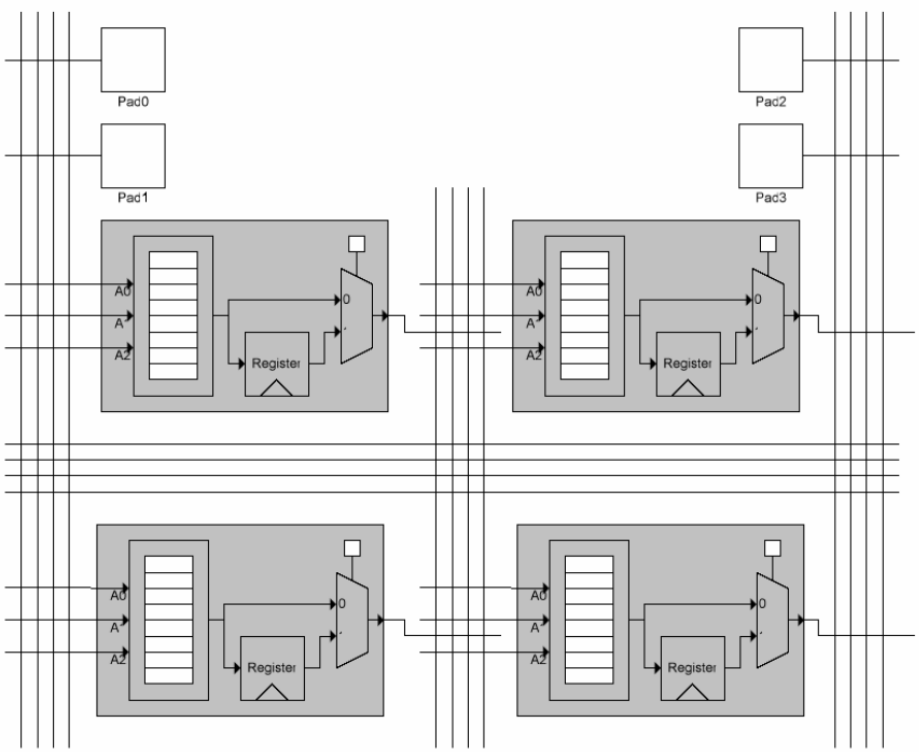
1. [25 points] Shown below is an example LE from an FPGA where the configuration bits are filled in to implement a NAND gate. Notice that not only is the 3-LUT filled in, but the control bit for the MUX is set.



Your objective is to implement the following circuit into the FPGA fabric shown below using the **minimum** number of logic elements.



Fill in the white boxes with either 1 or 0 to indicate both the programming of the 3-LUTs and the MUX control bits. Indicate connected wires with an X. In addition to configuring the LEs, you must make sure to route all the signals you use, including Reset, and to configure the four I/O pads at the top. Each signal that connect to the outside world must be connected to an I/O pad. Reset is the only input and the three bits ($c_2c_1c_0$) are the only outputs. In the white I/O pad box, write in the name of the signal connected to it. Each I/O pad would be connected to a pin on an FPGA chip.



2. [25 points] Consider a four-input LUT (used for example in the Altera Cyclone II device). This LUT can implement any Boolean function of four variables. Consider the function

$$Z = A \cdot (B + C) + B \cdot D + E \cdot F \cdot G \cdot H \cdot I$$

We can use four LUTs to implement Z as follows.

LUT1: $Z = Z1 + B \cdot D + Z3$
LUT2: $Z1 = A \cdot (B + C)$
LUT3: $Z3 = E \cdot F \cdot G \cdot Z5$
LUT4: $Z5 = H \cdot I$

a. [10 pts] What is the critical path length?
b. [15 pts] Find a better assignment in terms of area and critical path.