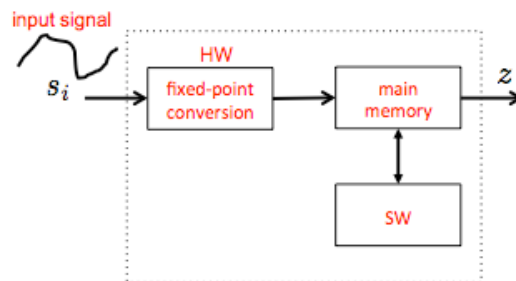


1. [5 points – team work not allowed] Given the two decimal numbers 9.25 and 4.625:
 - a. [2 points] Transform these two numbers to binary assuming a floating point format with 4 bits for the exponent part, 5 bits for the fraction and a bias of 7.
 - b. [2 points] Add the two numbers in binary.
 - c. [1 point] Convert the addition results from binary to decimal and verify that your solution is correct.

2. [10 points] A designer is asked to design a system that samples an analog input signal, s_i , and computes the result $z = (s_1 + s_2) \times (s_3 + s_4)$ for every four consecutive samples. To realize the system, the designer created a reconfigurable system that consists of HW components and SW components as illustrated in Figure 2. The HW component consists of a single floating-point to fixed-point converter, which samples the input signal and stores the resultant samples in fixed-point representation in the main memory as illustrated in the figure. The fixed-point representation is 8-bit total with 2 bits for the fractional part. The SW component, which executes on a 32-bit soft processor, is a simple SW routine that reads the samples from the memory and computes z .



- a. (2 points) Assuming that the integer part of the input signal s_i is always between 0 and 32, let the error introduced by the HW in converting s_i to fixed-point representation be denoted by e_i . What is the worst-case value of e_i ?
- b. (6 points) Derive a formula that gives the final error in the system output z as a function of HW errors, e_i , and the inputs s_i . What is the worst-case value of the error in z ?
- c. (2 points) Because of some unfortunate event, the addition operation in SW is producing in- accurate results that are input dependent. Do the SW and HW errors add up independently in the final system output z ; i.e., can we say that the final error in z is equal to HW-related errors + SW-related errors? Elaborate on your answer.

3. [35 points – team work not allowed] The objective of this HW is to get you acquainted with the basic skills required to work with the Nios II processor systems. Before you attempt this HW, **please make sure to follow the Nios II tutorial that is available on the class webpage before you attempt this LAB.**

This game is used to tune brain recognition skills. In the game, The DE2 board is possessed by an alien. It flashes some alien symbol (see example below) once on the 7-segment display that is on the extreme left, and then it displays four symbols on the four 7 segment displays at the extreme right. Your objective is to choose (via the push buttons) the number (or location) of the symbol that matches the alien symbol. You have to be quick because the board will only give you 3 seconds to make your choice (display the timer on one of the remaining 7 segments). A green LED should turn on if you match successfully; otherwise, a red LED should turn on. For this exercise, you should be designing your circuit using the QSys system, which allows the Nios II processor to interface directly with the push buttons and the LEDs. The functionality of the lab should be entirely based on the C code (no Verilog) that you will write and compile for the game. The game should terminate after 10 iterations, and then display a count of the number of successful recognitions.

Example of an alien 7-segment symbol:

```
  |
  |
  |
  |
  |
  |
  |
```

You can make an align symbol by turning on randomly some of the bars in the 7-segment.

Deliverables include:

- Email: project file
- Written documentation includes:
 - Report the amount of logic and routing area utilized in the FPGA
 - Snapshot of the final layout of the FPGA as produced by the synthesis tool
 - C code and memory size it takes after compilation
- 5 points will be allocated to games that work smoothly in an entertaining manner.
- The team that produces the code that uses the smallest amount of memory gets 5 extra bonus points that can be used towards any lab/hw.