Brown University
School of Engineering
EN2911X Reconfigurable Computing.
Prof. Sherief Reda
HW/LAB 07 (20 points). Due Date: Friday, Oct 31st 2014.

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1. (20 points) The following functional description of a data flow graph is given:

$x1 = (a1+a2)+a1$
$out1 = (x1 + x1)*(a3 * a4 + a5)$
$out2 = (a6 * a6 + a7)*a8$

An addition or multiplication operation requires one clock cycle.

a) (5 points) Conduct an ASAP scheduling and draw the corresponding scheduled data-flow graph. What is the minimum latency (Tmin)? How many adders and multipliers are needed?
b) (5 points) Given that the latency is Tmin, conduct an ALAP scheduling sand draw the corre- sponding scheduled data-flow graph.
c) (5 points) What is the minimum number of resources (adders and multipliers) needed to achieve Tmin latency? Draw the scheduled data-flow graph (DFG) that uses such minimum number of resources.
d) (5 points) Sketch the circuit that synthesizes the DFG of part (c). Determine the size of all required steering multiplexors. Clearly enumerate the control signals required for the circuit, and accordingly determine the content of the control ROM.