High-Throughput TSV Testing and Characterization for 3D Integration Using Thermal Mapping

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ABSTRACT

We propose a new framework to detect structural defects and characterize the variability in the electrical resistance of through-silicon vias (TSVs) in 3D ICs. Our method offers a number of advantages that have been hard to achieve in the past. In particular, the proposed framework provides high throughput TSV testing at pre-bonding stage. A resistive liquid electrode is placed at the back side of the device to conduct electric current from TSVs. The current passing through TSVs leads to heat generation which can be captured by a remote, high-sensitivity thermal camera. The captured thermal signatures from the TSVs are then contrasted against reference thermal maps generated from known good die and/or electro-thermal simulations of models of good TSVs. A proposed automatic classification technique is capable of determining the status of TSVs based on their thermal signatures. We demonstrate the viability of the proposed technique using extensive simulation results on realistic TSV configurations.

ACM Categories & Subject Descriptors
B.8.1 [Performance and Reliability]: Reliability, Testing, and Fault-Tolerance.
General Terms: Reliability, Measurement, Performance.
Keywords: TSV testing, 3D ICs, thermal imaging.

1. INTRODUCTION

3D Integration with through-silicon vias is a promising technology that enables a number of improvements to electronic devices, including higher communication bandwidth, less communication power, higher integration density, and smaller form factor [4]. Despite these advantages, 3D integration faces a number of challenges including high spatial power densities and testing. Testing is a specially important issue, as it determines the eventual cost and acceptance of the technology [12, 5]. 3D integration offers a unique testing challenge, as full testing of TSVs is difficult to achieve before bonding [9, 6], and post-bonding testing implies the possibility of packaging a good die with a faulty one, reducing the overall yield [10]. There is real need for pre-bonding test and characterization mechanisms that can enable high-throughput, reliable detection of TSV connectivity status.

In this paper, we propose a new paradigm for pre-bonding TSV testing and characterization using thermal imaging. Thermal imaging is an established technique for fault diagnosis in regular integrated circuits [2]. Our work extends the potential of this approach for the first time to TSV testing. The contributions of our paper are as follows.

1. We propose a new framework for pre-bonding TSV testing, where thermal imaging is used to test the electrical connectivity of TSVs. By using a resistive electrolyte solution on the back side of the device (*e.g.*, in die or wafer form), electrical current can pass through the TSVs and solution. Heat generated from the current can be picked up by a thermal imaging equipment. The captured thermal signatures can be used to analyze whether a TSV is defective or operational, and can provide characterization information about defects.
2. To analyze the thermal signatures from a device, it is necessary to establish a *reference* thermal map, either through measurements on known good dies or through design modeling. We propose a finite element based electro-thermal modeling and simulation technique to establish the reference map.
3. To classify the status of TSVs, we propose a classification technique that takes as inputs the thermal signatures from the device under test and the thermal reference map, and automatically detects functional and defective TSVs using statistical clustering methods.
4. As a proof of concept, we simulate a test-design with 100 TSVs. We elucidate the tradeoff in TSV testing accuracy as a function of the number of faulty TSVs. We also demonstrate the ability to characterize some types of defects based on thermal signature.

The organization of this paper is as follows. Section 2 overviews previous related work in TSV and 3D IC testing. In Section 3, we describe our main proposed framework based on thermal imaging. In Subsection 3.1, we describe the main ideas for our electro-thermal modeling and simulation method, and we describe in Subsection 3.2 our proposed automatic classification technique. Our simulation results are provided in Section 4. Finally, Section 5 provides the main conclusions and future directions for this work.

DAC '13, May 29 - June 07 2013, Austin, TX, USA.

2. RELATED WORK

Assembly of 2D ICs to build 3D ICs has become a reality and has potentially cleared the roadblock for keeping the momentum of Moore's law going. However, the 3D ICs would require modifications in all stages of the chip design. For example, the existing design for test methodologies might have to be supplemented with extra testing steps to address the new types of faults introduced from additional manufacturing steps required for fabricating 3D ICs. Therefore, testing 3D ICs is more challenging than testing 2D ICs due to increased complexity and higher testing cost of 3D ICs [5]. A typical 3D IC would have thousands of TSVs embedded in the substrate to provide electrical connection between stacked dies. The fabrication of these TSVs with high yield is still an active area of research in the fabrication community. It is typically cost effective to identify dies with defective TSVs early in the process to save the un-necessary cost incurred by later steps on defective dies [7].

To this end, a number of test and DFT solutions have been proposed to test the quality of TSVs at different stages of the manufacturing process; these include pre-bonding, post bonding and post-packaging stages [3, 9]. While Chi *et al.* proposed strategies to test ICs at post-bonding stage [3], Noia *et al.* implemented a new test-architecture in the logic to enable the testing and characterization of TSVs at pre-bonding stage [9]. It is generally assumed that all TSVs are controllable and observable through dedicated scan flip flops. The architecture proposed by Noia *et al.* would require probe tips to come in contact with TSVs. However, our proposed technique is based on imaging the die-surface and hence, the potential risk of TSV damage from probe tips is eliminated. Our technique requires to generate a simple test-pattern to put alternate TSVs at ground and V_{dd} potential using the scan flops available for each TSV.

While Smith *et al.* present a probing technology that could be used for probing TSVs with finer pitch [11], the possibility of implementing RF-based wireless techniques to test chips at both die and wafer levels has also been explored [6, 8]. In particular, laser direct testing techniques, currently used to detect defects in PCBs, could be used for contact-less testing of 3D ICs [6]. However, the laser based testing would be a slow process due to its inherent sequential nature. In this paper, we propose a high-throughput technique to test and characterize TSVs in a 3D IC at pre-bonding stage. The technique requires no expensive and potentially damaging mechanical contact to the TSVs. It does require a modest number of contacts to the front side of the die through existing test pads.

3. PROPOSED FRAMEWORK

We propose a new framework for testing and characterization of TSVs without requiring any form of bonding. In our framework, which is illustrated Figure 1, the back side of the wafer with exposed TSVs is contacted with a liquid that acts as a single backside electrode. The other side of the liquid is in contact with an infrared-transparent window. The infrared-transparent window has two functions: (i) it mechanically supports the wafer, and (ii) it allows transmitting of thermal emissions from the wafer side. The liquid has finite resistivity (to avoid electrical short among TSVs) so that electrical current flowing through the liquid will generate heat. A pattern of voltages is applied to the TSVs either directly through automated test equipment (ATE) contacting the wafer from the front side or through the use of scan chains or built-in self test. Current is conducted through the liquid from the TSVs that are at high voltage to the TSVs that are at ground. The induced current causes localized heating around the good TSVs due to spreading resistance. Open or highly resistive TSVs will not conduct current and no localized heating will be generated. The localized heating around good TSVs will cause temperature gradients, which can be measured by thermal imaging equipment viewing the liquid-window interface through the window. By comparing the measured steady-state thermal image from a device under test to a *reference steady-state thermal image* of a die with all good TSVs, we can pinpoint any open TSVs. Furthermore, modern thermal imaging cameras have thermal sensitivity of about 20 mK [1], which is less than the temperature difference caused by the induced current, as we will show below. Thus, by inspecting the strength of thermal emissions, we can characterize the resistance of the TSV.

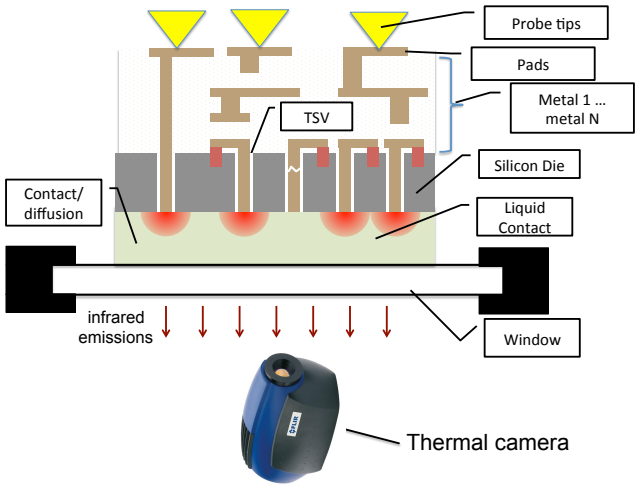

Figure 1: Proposed framework for high-throughput testing of TSVs at pre-bonding stage.

The key element of our method is to provide a liquid electrode that has finite resistivity and that makes good electrical contact to the TSVs. Water-based electrolyte solutions can satisfy these requirements, as elaborated later in Section 3.1. We believe that electrochemically deposited compounds on the TSVs should be negligible or easily removable with a simple rinsing step. Furthermore, the liquid electrode and the infrared-transparent window must have sufficiently low thermal conductivity to maintain the thermal gradients generated from the flow of electrical currents. For these reasons, we utilize water-based solutions and a chalcogenide glass window in our setup. We assume that all TSVs can be set to a high or low voltage state. This is obviously true for TSVs connected to the power rails. Digital I/O lines can be set high or low via scan-in and/or BIST mechanism. If some TSVs are strictly inputs, continuity can still be tested by applying a bias voltage to the liquid electrode and inducing current through ESD diodes connected to the pins.

To illustrate the operation of the proposed technique, we construct a simple test case. We assume that there are only five TSVs, arranged in a diamond pattern with the center TSV connected to V_{dd} (1V) and the surrounding four TSVs are connected to ground as illustrated in Figure 2.a. Using modeling and simulation techniques (described in Section

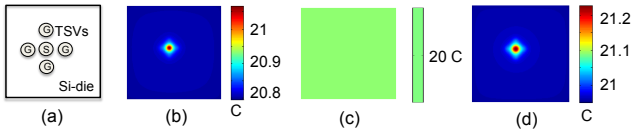

Figure 2: (a) A die with 5 TSVs arranged in the diamond pattern; (b-d) thermal-profiles at the top of ion solution: (b) when the center TSV is at 1V and other TSVs are at 0V, (c) when the center TSV is open and non-conductive, (d) same as (b), but the diameter of the center TSV is increased by 30%.

3.1), we provide the simulated thermal profile at the top of ion-solution in 2.b. (For simplicity, we refer to the window/ solution interface as the "top" even though it appears at the bottom in Figure 1.) If the center TSV is defective, say completely open, then there is no current in any TSV and therefore the top surface of ion-solution will be at ambient temperature (20 C), as shown in Figure 2.c. Thus, we can obtain a thermal image by simulation of the good-TSV case and contrast this image to the thermal map captured from the actual die, and use the difference to test TSVs.

Next, we characterize the variability in the diameter of the center TSV. To that end we assume that all TSVs are conducting, but the center TSV has a smaller or larger diameter than nominal. Figure 2.d shows the thermal image of the top of the ion-solution when the diameter of the center TSV is 30% higher than its nominal value. We notice that the temperature at TSV location increases with increase in diameter of the TSV. This is because the increased diameter of the TSV at the liquid interface decreases the spreading resistance in the liquid, leading to more joule (V^2/R) heating in the vicinity of the TSV.

Our proposed method offers a number of advantages over current methods:

1. Scalability and Throughput. A thermal infrared camera can capture the thermal signatures of large fields of view spanning few mms with 3-5 μm resolution. Thus, our method can capture the status of several hundreds or even thousands of TSVs in parallel at the same time in a single image, enabling high-throughput testing. The size (few micron) and pitch (few 10s of microns) even in aggressive TSV roadmaps are resolvable by state-of-the-art short-wave and mid-wave infrared cameras.
2. Testing Cost: Our method requires standard thermal imaging equipment [5]. Further, only low-bandwidth ATE should be required to front-side contact of the device's power rails, ground, and some scan chain inputs. Thus, our setup eliminates the need for large number of pin contacts and pin electronics per TSV.
3. "Non-contact" nature: Although probe-technology has improved significantly in recent years [11], the problem of TSVs' ends becoming damaged from probe tips still exists. However, the proposed technique enables high-throughput testing of TSVs in a "contact-less" manner.

In the rest of the paper, we explain in details the model and simulation techniques required to generate the reference thermal map, together with techniques for automatic classification of TSVs.

3.1 Electro-thermal Modeling

Model Setup: Our proposed technique relies on capturing the thermal image of the die when electric current flowing in TSVs generates heat in the liquid contact solution. The thermal profile at the surface of the die depends on the location and number of TSVs that conduct electrical current. By applying a test pattern to the TSVs of the die under test, we can detect the defective TSVs immediately by comparing the measured thermal-profile with the thermal-profile of the die with good TSVs. In order to verify the feasibility of the proposed technique and also to perform comprehensive study of the proposed idea, we built a simulation model of the system using a well known Multiphysics simulation-software, COMSOL. The software has a finite-element based numerical solver as its core computational engine.

In order to solve the modeling problem using finite-element method (FEM), the complete geometry of the arrangement given in Figure 1 has to be divided into smaller elements in a process known as meshing. Creating a proper mesh is important for two reasons: (1) a properly-sized mesh enables accurate simulation of the required physical phenomena; and (2) it controls the convergence of the numerical solution. For these two reasons, we refined the mesh to appropriate sizes at different interfaces and corners by adding boundary-layers and by choosing the mesh-size individually for each domain. The mesh is refined iteratively until it has insignificant impact on the final solution.

In the proposed setup, we use a thin layer of electrically conductive ionic solution at the backside of the die, *i.e.* at the side where TSVs are exposed after substrate thinning. The ion solution is used to provide reliable path for the electric currents flowing among different TSVs when one side of the TSVs are applied with special test-patterns. Further, to keep the ion solution in place and for mechanical support, we put an infrared transparent window on top of the solution. The window material is chosen such that it is not only IR-transparent, but also has low electrical and thermal conductivities. The low thermal conductivity of the window ensures that the temperature gradients (distinguishable cold spots) generated at the top of ion-solution due to defective TSVs are not washed-out by the window. Similarly, the electrically non-conductive property of the window material helps in limiting the flow of electric current entirely inside the solution, which in turn generates detectable thermal hot spots inside the solution and exactly at the locations where TSVs are present. We propose using a state-of-the-art infrared camera to capture the thermal image at the surface of the ion-solution.

The properties of different materials used in our model are reported in Table 1. Mainly, the model has five different materials: silicon-die, copper-TSVs, ion-solution (e.g. NaCl solution with appropriate electrical conductivity), chalcogenide glass as an IR-transparent window, and air as ambient. Here, ρ denotes the density of the material in kg/m^3, k represents the thermal conductivity of the material in W/(m.K), C_p denotes the specific heat capacity of the material at constant pressure in J/(kg.K), ϵ_r represents the relative permittivity of the material, and σ denotes the electrical conductivity of the material in S/m. We assume that the ionic solution has the same heat capacity as pure water.

Model Simulation: In order to compute the thermal-profile of the system, essentially, we have to solve Joule heating from electrical currents and heat-transfer physics

Material properties	ρ (kg/m^3)	k (W/m.K)	C_p (J/kg.K)	ϵ_r	σ (S/m)
Silicon	2330	148	703	12.1	1e-12
Copper	8700	400	385	1	5.998e7
Ion-solution	1041.3	0.56	3930	81	5-10
Chalcogenide	4410	0.24	330	5.19	1e-9
Air	1.2041	0.024	1003.5	1	0

Table 1: Material properties, where the terms ρ, k, C_p, ϵ_r, and σ are defined in the text.

simultaneously. In particular, we solve the following set of steady-state equations using a finite-element solver to compute electric current density in the geometry:

$$\nabla.\mathbf{J} = Q_j \tag{1}$$

$$\mathbf{J} = \sigma\mathbf{E} + \mathbf{J}_e \tag{2}$$

$$\mathbf{E} = -\nabla V \tag{3}$$

where $\mathbf{J}$ denotes the current density in A/m^2, Q_j represents the current source in A/m^3, $\mathbf{E}$ denotes the electric field, $\mathbf{J}_e$ denotes the external current density in A/m^2, V represents the electric potential in Volts and ∇ is the differential operator in space domain. Here, Equation (1) denotes the current-continuity equation; Equation (2) is Ohm's law and Equation (3) relates electric potential and electric field under static conditions. We assume that the complete setup is placed in air and therefore, we apply electrical insulation boundary-conditions at all surfaces that are exposed to air. This is equivalent to setting $-\hat{n}.\mathbf{J} = 0$, where $\hat{n}$ is the unit normal-vector pointing outward to the boundary. Applying ground or non-zero potential at any TSV is equivalent to setting $V = 0$ or $V = V_{dd}$, respectively, at that surface, where V_{dd} is any non-zero voltage.

For simulating heat-transfer in the system, we solve the steady-state heat diffusion equation in COMSOL:

$$-\nabla.(k\nabla T) = Q, \tag{4}$$

where k is the thermal conductivity of the material, T is the temperature in Kelvin, and Q denotes the heat sources/sink in W/m^3. For Joule heating, as is the case in our system, Q comes from the resistive heating and is equal to I^2R/vol, where I is the electric current, R is the electric resistance of the material, and vol is the volume of the meshed element. Further, we assume that the net thermal resistance of the reference die plus liquid and window assembly to ambient is equal to 10 K/W; this is consistent with values we have observed in the lab with similar setups, and is far larger than in commercial heat sinks for microprocessors which have less than 1K/W thermal resistance. For all simulations, we use 20 C as the ambient temperature in this paper.

In our setup, we capture thermal profile of the system in steady-state. Our simulations show that devices reach thermal steady-state within 1 second; since the data acquisition time can be significantly less than 1s per image, the acquisition time per capture is on the order of 1s.

3.2 Automatic TSV Classification

In order to test and characterize all TSVs simultaneously, we apply in simulation a test pattern to all TSVs such that TSVs are either at ground or V_{dd} potentials. The application of any desired test pattern is possible because all TSVs would have scan flops associated with them for design for testability purposes. Hence, each TSV is both controllable and observable through boundary scan flops. We simulate the thermal profile at the surface of the ion-solution for a good die, and denote the corresponding thermal-profile as our reference thermal-image. We store this image and use it for testing all dies of the same configuration, *i.e.* same layout and dimensions for TSVs and substrate. To test any die with the same configuration, we apply the same pattern to all TSVs and capture thermal image of the top surface of the ion-solution using an infrared camera. Next, we subtract the reference thermal-image from the captured image. For example, if only one TSV is defective in the die, then that TSV would not carry any current and therefore there will not be any localized heating in the TSV and in the vicinity of this TSV in the ion-solution. Hence, it will be possible to detect the location of the defective TSV. It is worth mentioning that all TSVs, whether connected to ground or V_{dd} will carry electrical currents and generate heat, as long as they are not defective. When all TSVs are conducting, the temperature at all locations in the die would be higher than when one or more TSVs are non-conducting. Hence, the difference-image would have lower pixel values in the regions corresponding to defective TSVs. The more the number of defective TSVs in the die-under test, the higher would be the magnitude of temperatures in the difference-image. However, if the number of defective TSVs is large, it might become difficult to detect the cold-spots due to interaction between different TSVs through lateral heat diffusion.

We propose a fully automated process to identify, locate, test, and characterize the defective and good TSVs in the die. We use a standard k-means classification based method on the difference-image to classify the TSVs into two bins: good TSVs and defective TSVs. To this end, we divide the thermal image of the entire die/ion-solution-top-surface in to multiple areas, equal in number to the total number of TSVs in the die. Thus, each TSV will be represented by a multidimensional vector that represents its thermal signature; the dimension of the vector is equal to the number of pixels assigned to each TSV in a thermal map, where each pixel denotes a temperature value in the thermal map. We assume that all the TSVs have the same nominal diameter. Therefore, each TSV is represented by the same number of pixels in a thermal map. Also, the number of multidimensional vectors will be equal to the total number of TSVs in the die. These vectors are given as inputs to the k-means classifier to classify them into two bins. As confirmed by the simulation results (presented in Section 4) on a test-die, the k-means algorithm has very good classification performance.

We use two metrics for measuring the accuracy of the classified TSVs: *detection accuracy* and *true-positive rate* (TPR). The detection accuracy is computed by taking the ratio of true detection (sum of the number of good TSVs classified as good and the number of defective TSVs classified as defective) to the total number of TSVs in the die. The TPR is defined as the ratio of number of defective TSVs that are classified as defective to the total number of defective TSVs in the die. The k-means classification method used in this paper is a non-supervised method and therefore, there might be a scope of improving the detection-accuracy by building a new classifier with the help of training data.

Further, if TSVs have different diameters or different resistances than nominal, this would lead to differences in the associated thermal hot spots in the liquid, as explained in Section 4.

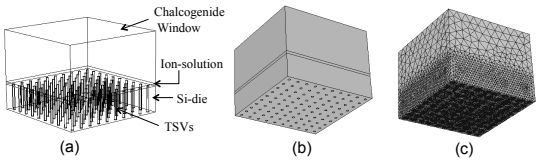

Figure 3: (a) Simulation model showing 100 TSVs, (b) un-meshed geometry, and (c) meshed geometry of the simulated model.

4. SIMULATION RESULTS

Setup Details: For our simulations, we assume the following dimensions for different domains of the system. The diameter, length, and pitch of good TSVs are assumed to be 5 μm, 50 μm, and 20 μm respectively. Thickness of the silicon die is kept the same as the length of TSVs because, before bonding two dies, the substrate is thinned until the TSVs are exposed. The thickness of the resistive ion solution is kept as 5 μm; a typical ion-solution that could be used in our setup is a solution of Sodium Chloride (NaCl) salt in water. Resistivity of the solution could be varied by changing the concentration of NaCl. We use 3% NaCl solution in our setup that has electrical conductivity of about 5 S/m. Fortunately, the NaCl solution has low thermal conductivity, which helps in maintaining the spatial gradients in the solution when good TSVs are carrying current and defective TSVs are non-conducting. Also, we use an IR-transparent chalcogenide glass window at the top of ion-solution for practical purposes as illustrated earlier in Figure 1. The temperature dependent infrared radiations generated from the top of ionic solution pass through this window before they are captured by the camera.

The geometry of the modeled system is shown in Figure 3.a; it shows 100 copper TSVs (10x10) fabricated in a 2-D grid pattern over the die-area. Figure 3.b and Figure 3.c show the un-meshed and meshed geometries of the system, simulated using a commercially available numerical solver. Moreover, appropriate boundary conditions and heat transfer coefficients are used at all surfaces of the system to approximate the real system.

TSV Testing: In order to test TSVs of the die, we use the technique described in section 3.2. We first simulate the reference thermal-profile profile at the top of the ion-solution when all 100 TSVs are non-defective. The simulated thermal-profile is shown in Figure 4.a; it represents the reference thermal image for the good die. Next, we simulated a few cases when multiple TSVs (selected randomly) are defective; in particular, we simulated the thermal-profiles when multiple TSVs are open, and hence, not conducting any current. For example, Figure 4.b shows the thermal profile when two TSVs, located at (3,7) and (7,10) coordinates in the x-y plane, are open. Similarly, Figure 4.c to Figure 4.f show the simulated thermal images at the top of ion-solution for cases when 4, 8, 16, and 32 TSVs are open respectively. It is worth mentioning again that in all cases we apply ground and 1V potential at all alternate TSVs, but the TSVs that are open do not carry any current and therefore, we have lower temperature at those locations.

Next, as described in Section 3.2, in order to automatically detect the location of faulty TSVs, we subtract the reference thermal-image (shown in Figure 4.a) from test thermal images. The images after taking the difference between reference thermal-image and test-images for different faulty-

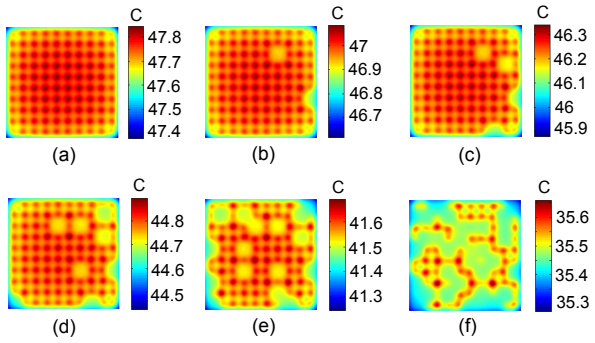

Figure 4: (a)-(f): Thermal maps when 0, 2, 4, 8, 16, and 32 TSVs are defective (open).

TSVs cases are shown in Figure 5. We simulated all cases, wherein any number of TSVs (0 to all) are defective. Figure 5.a to Figure 5.f show the difference-images for the cases when 2, 4, 8, 16, 32, and 64 TSVs (selected randomly) are assumed to be defective at a time. For a real system, the test images could be captured using a high-sensitivity thermal-imaging camera. The reference thermal-image could be obtained by either simulations or from the measurements on a known good die, whose all TSVs are non-defective. It is clear from Figure 5 that the difference image has lower temperature at locations corresponding to defective TSVs than at locations where good TSVs are located. For example, the difference in the mean temperature at locations above defective TSVs and the mean temperature at locations above good TSVs is more than 100mK when 32% of the TSVs are defective and it could be easily detected by the state-of-the-art mid-wave infra-red cameras, which have noise equivalent temperature difference (NETD) of about 20 mK. Based on the simulation results, we observe that the temperature gradients are higher than the NETD of IR cameras, even when 50% of the TSVs are defective.

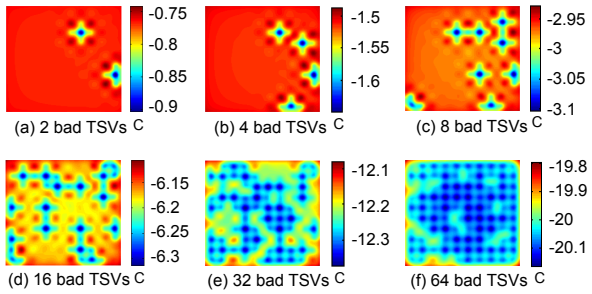

Figure 5: Difference between measured and true thermal maps when 2, 4, 8, 16, 32, and 64 TSVs are defective (open).

As described in Section 3.2, for automatic detection of faulty TSVs, we divide the difference thermal image into 100 different groups, leading to a thermal signature per TSV, and use k-means classification method to classify good and defective TSVs for each test-case. To verify the effectiveness of the proposed classification technique, we simulated the thermal profiles of the die by increasing the number of defective TSVs progressively from 1 to 100. We computed the true positive rate (TPR) and the detection accuracy for each case. Figure 6.a gives the TPR of our detection method as a function of the number of faulty TSVs. It is clear that

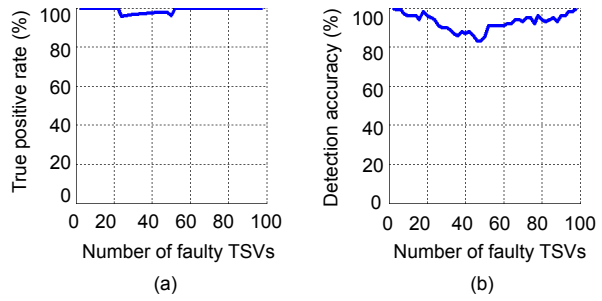

Figure 6: (a) True positive-rate (TPR), (b) Detection accuracy of the TSV classification using k-means clustering algorithm.

our proposed detection technique is able to detect the defective TSVs almost all the time. Further, as could be seen from Figure 6.b, the overall detection accuracy is quite high (>80%), even when 50% of the total number of TSVs are defective in the die. The results show that our proposed technique is not only fast and scalable, but also is very reliable in detecting the faulty TSVs in the die.

Characterizing Variations in TSV Diameters and Resistance: For simulating the characterization process, we performed two studies. First, we simulated the effect of a central TSV in the 100-element array having a diameter change of up to +/- 30% from nominal. Figure 7.a shows the resulting peak temperature vs. TSV diameter. As expected, larger diameters lead to lower spreading resistance and larger temperature peaks due to joule (V^2/R) heating. Every 10% change in diameter caused about a 33 mK change in peak temperature, which is above the NETD of a thermal camera. Second, we simulated increased resistance of a TSV compared to nominal in a 5-TSV case as described in Section 2. The result is shown in Figure 7.b, where difference between the maximum and the minimum temperature of a thermal map is denoted by ΔT. When the TSV resistance becomes comparable to the effective resistance of the fluid (on the order of 25 kOhm in our simulation) the thermal signal decreases due to a decreased voltage drop across the fluid. This effect allows characterization of the resistance of a TSV compared to a threshold value that can be tuned by varying some parameters of the experiment, such as the resistivity of the fluid.

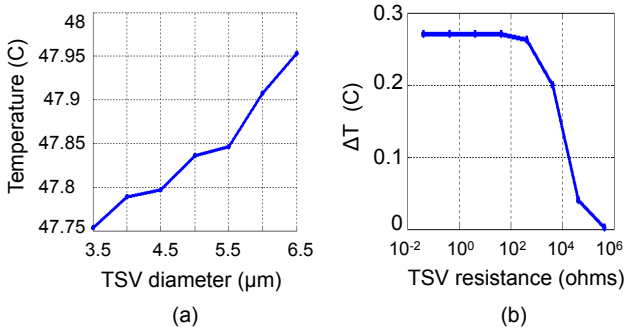

Figure 7: (a) Change in peak temperature due to variation in diameter of one of the TSVs for the die containing 100 TSVs. (b) Difference between the maximum and the minimum temperature of the thermal map (ΔT) when resistance of the center TSV changes due to partial defects for the die containing 5 TSVs.

5. CONCLUSIONS AND FUTURE WORK

In this work, we have proposed a novel and effective technique for high-throughput testing and characterization of TSVs in 3D ICs. In our method a high-sensitivity thermal camera is used to capture thermal signatures emitted due to heat generation from electric currents in TSVs. The thermal signatures are compared against a reference thermal image generated from simulation of a good device. We have proposed an electro-thermal simulation technique to generate the reference thermal map, as well as an automatic classification technique to analyze the differences between the thermal signatures and the reference map and to classify the status of TSVs. Simulation results show that our method is able to test TSVs and to characterize the resistance of TSVs.

Ongoing and Future Work. Our current method enables high-throughput testing of TSVs, but only one-by-one characterization. We plan to devise characterization techniques to analyze the resistances of multiple TSVs. This can be achieved through a combination of modeling and numerical inversion techniques, and/or through the use of multiple input patterns to the TSVs. In order to perform experimental validation of the proposed technique, we are also working on acquiring a representative TSV sample in our lab.

6. REFERENCES

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