

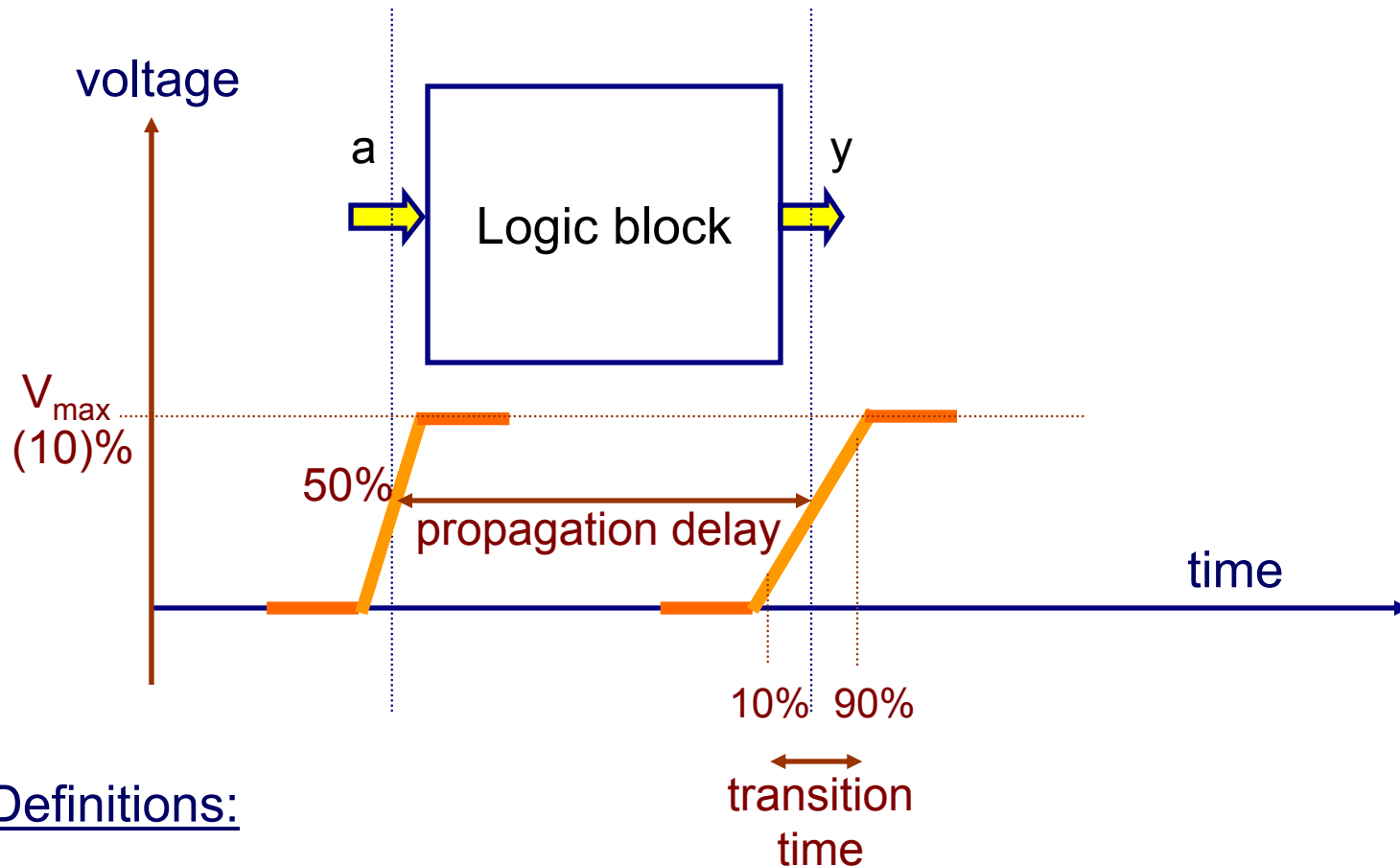
# Physical Design of Digital Integrated Circuits (EN0291 S40)

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Fall 2006

# Lecture 04: Timing Analysis

- Static timing analysis
- STA for sequential circuits
- Delay modeling: devices and interconnects
- Statistical static timing analysis

# Propagation delay definition



## Definitions:

- rise/fall *propagation delay*
- rise/fall *transition delay* (*slew (slope)*):  $\Delta V/\text{transition delay}$



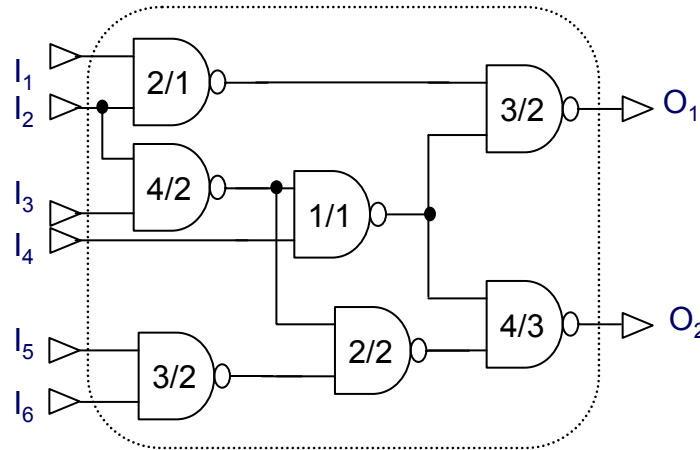
Problem: Given a circuit, find the path(s) with the largest delay (critical paths)

- Solution: run SPICE and report the results of the simulation
- Problem: SPICE is computationally expensive to run except for small-size circuits
- **WANTED:** We need a *fast* method that produces relatively accurate timing results compared to SPICE





# Finding the critical path through breadth first search

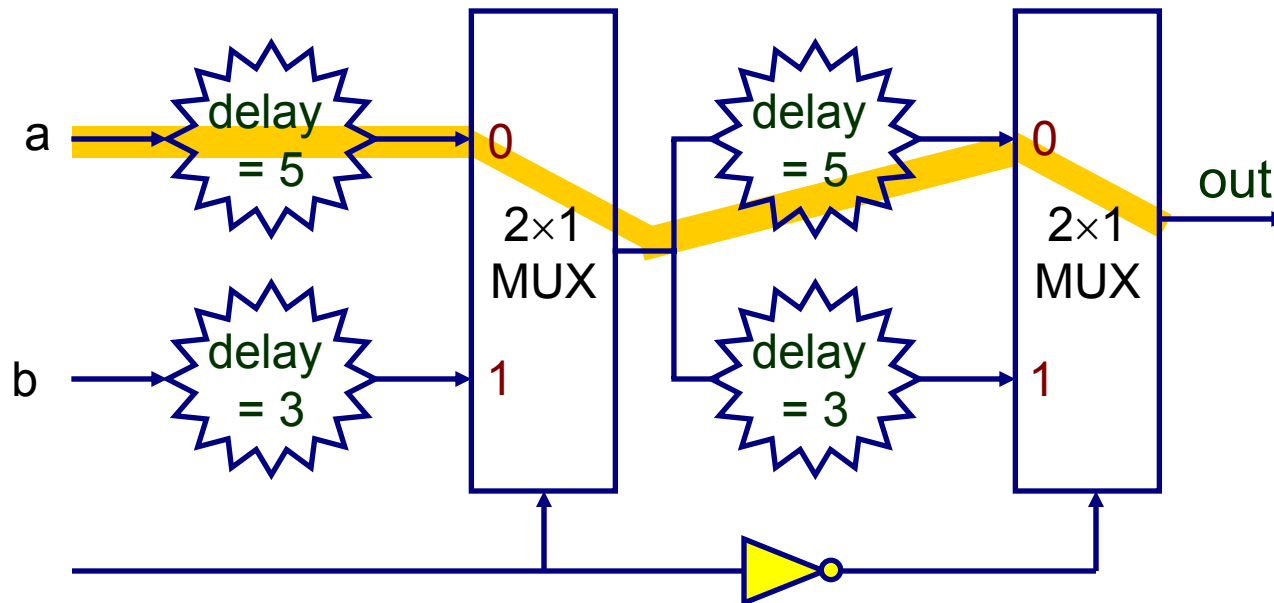


- Initialize queue  $Q$  to empty
- for all vertices  $i$  in  $V$ :  $nvisit[i]=0$ ;
- Add all primary input vertices to queue  $Q$
- While ( $Q \neq 0$ )
  - $i = \text{top of } Q$ ; remove  $i$  from  $Q$ ; computer delay of  $i$
  - for every edge  $(i, j)$ :
    - $nvisit[j]++$ ;
    - if( $nvisit[j] == fanin[j]$ ) add  $j$  to  $Q$



# STA can lead to false critical paths

- STA assumes a signal would propagate from a gate input to its output *regardless* of the values of other inputs



- What is critical path delay according to STA?
- Is this path realizable?  
No, actual delay is less than estimated by STA

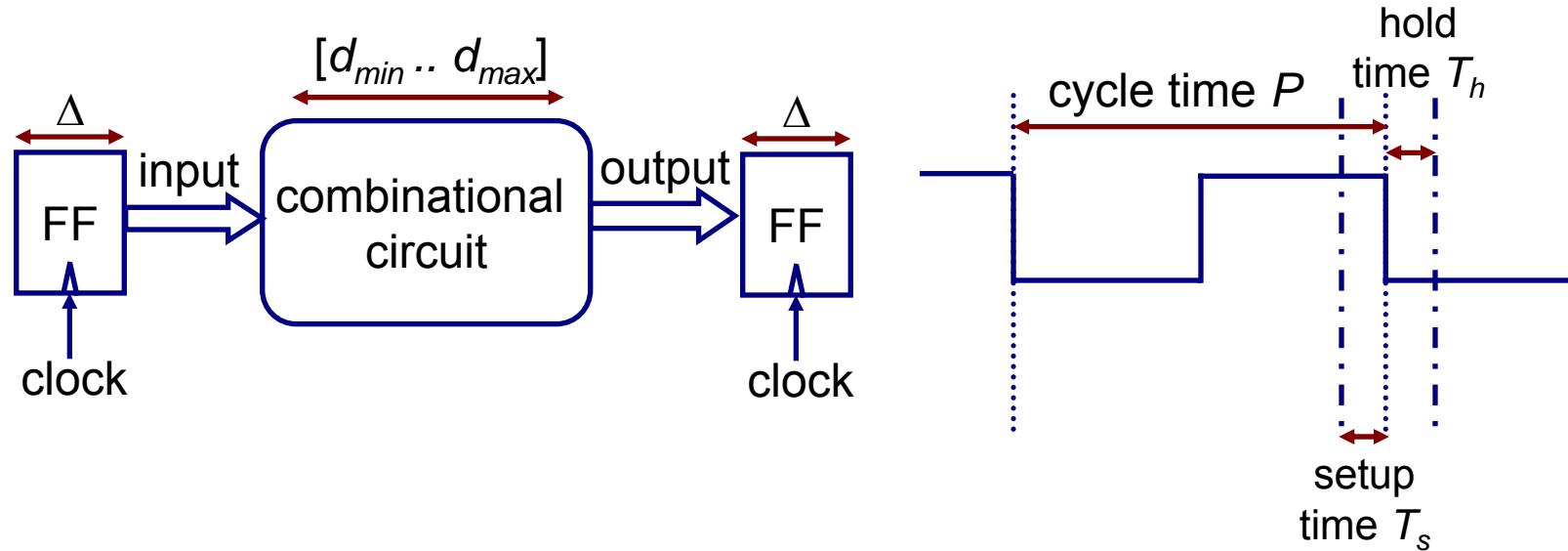
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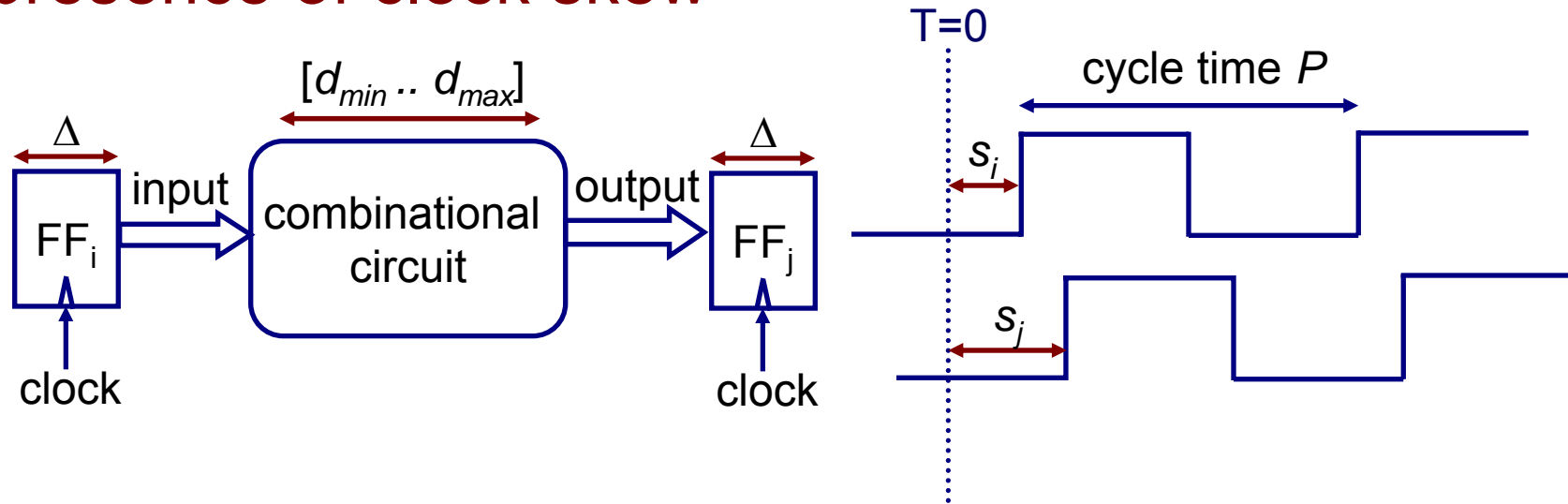


# Timing analysis of sequential circuits



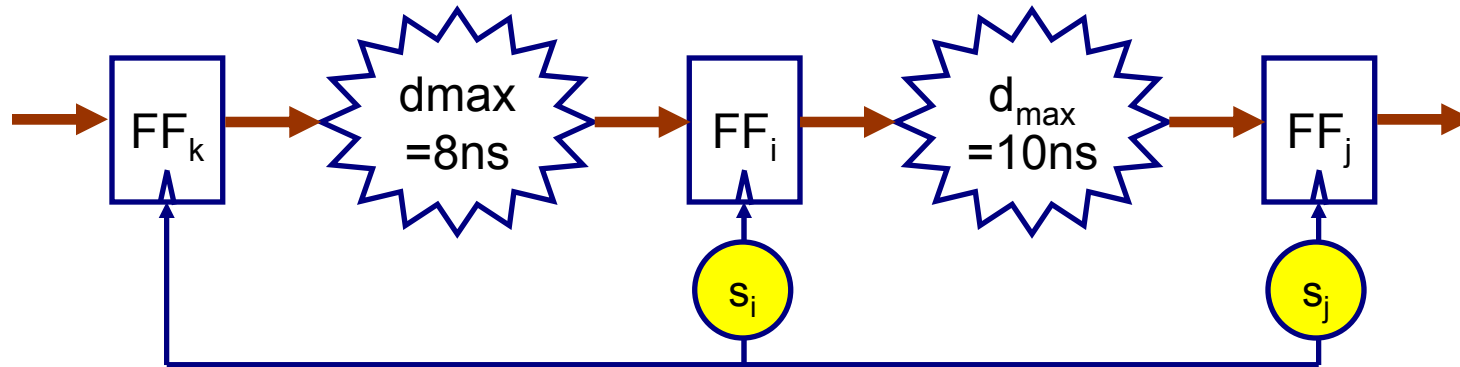
- $d$  is the propagation delay of a logic path
- $d_{min} \leq d \leq d_{max}$
- $\Delta + d_{max} \leq P - T_s$   
→  $d_{max} \leq P - T_s - \Delta$  (setup time constraint)
- $\Delta + d_{min} \geq T_h$   
→  $d_{min} \geq T_h - \Delta$  (hold time constraint)

# Timing analysis of sequential circuits under presence of clock skew



- $s_i$  and  $s_j$  skew of clock at FF  $i$  and  $j$
- $d_{min} \leq d \leq d_{max}$
- $s_i + \Delta + d_{max} \leq s_j + P - T_s$   
 $\rightarrow d_{max} \leq P - T_s - \Delta + s_j - s_i$  (setup time)
- $s_i + \Delta + d_{min} \geq T_h + s_j$   
 $\rightarrow d_{min} \geq T_h - \Delta + s_j - s_i$  (hold time)

# Sometimes introducing skew can be helpful



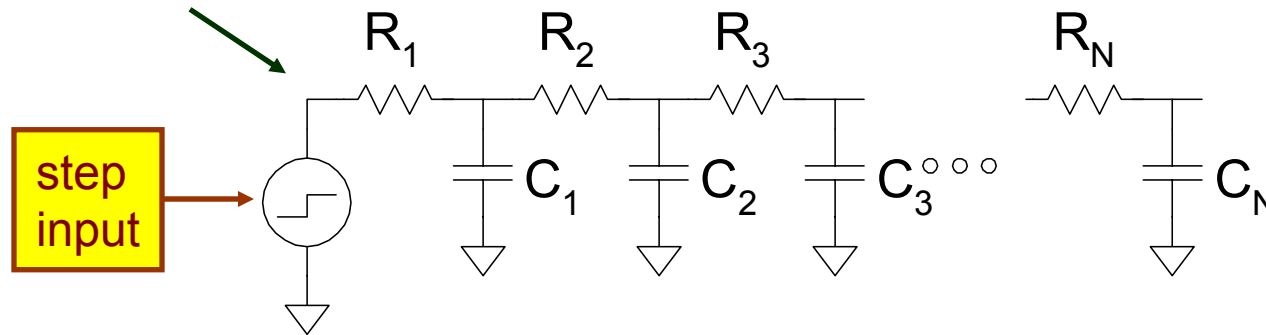
- Zero clock skew ( $s_i = 0$  &  $s_j = 0$ )  $\Rightarrow$  clock period = 10ns,  $f_{max} = 100MHz$
- $s_i = -1$   $s_j = 0$   $\Rightarrow$  clock period = 9ns,  $f_{max} = 111MHz$  (no timing violations)
- $s_i = -2$   $s_j = 0$   $\Rightarrow$  clock period = 8ns,  $f_{max} = 125MHz$  (no timing violations)
- Introducing skew also helps minimize the simultaneous switching of FFs  $\rightarrow$  less load on the P/G network
- STA is relatively easy once we figure out how to calculate gate and interconnect delay

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# Elmore delay model: An upper bound to actual delay in RC trees

any tree structure



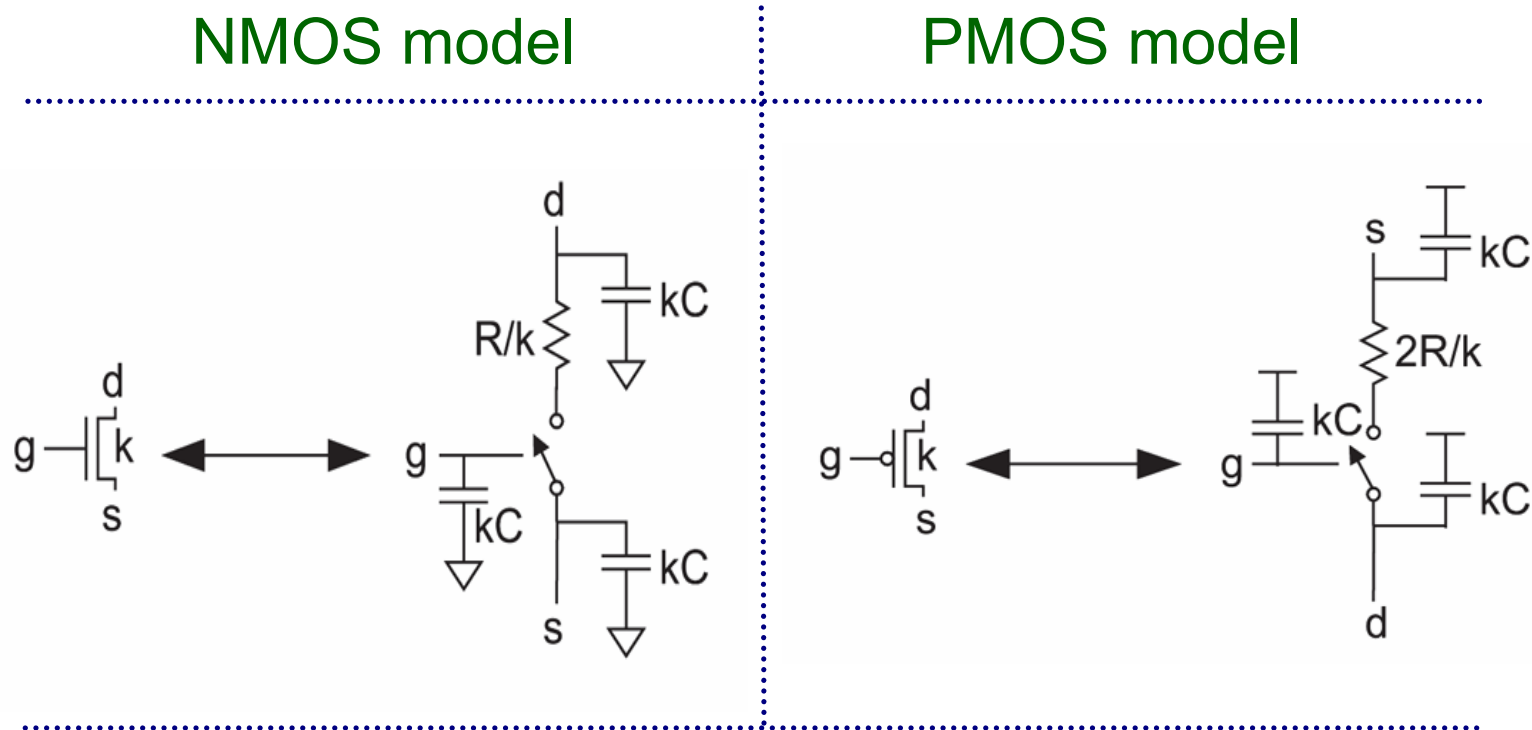
$$t_{pd} \sim R_1(C_1 + \dots + C_N) + \dots + R_N C_N$$

$$t_{pd} \sim \sum_{i=1}^N R_i \sum_{j \geq i} C_j$$

- Sum the result of multiplying each resistance by the capacitance down stream from it
- What is the runtime complexity?

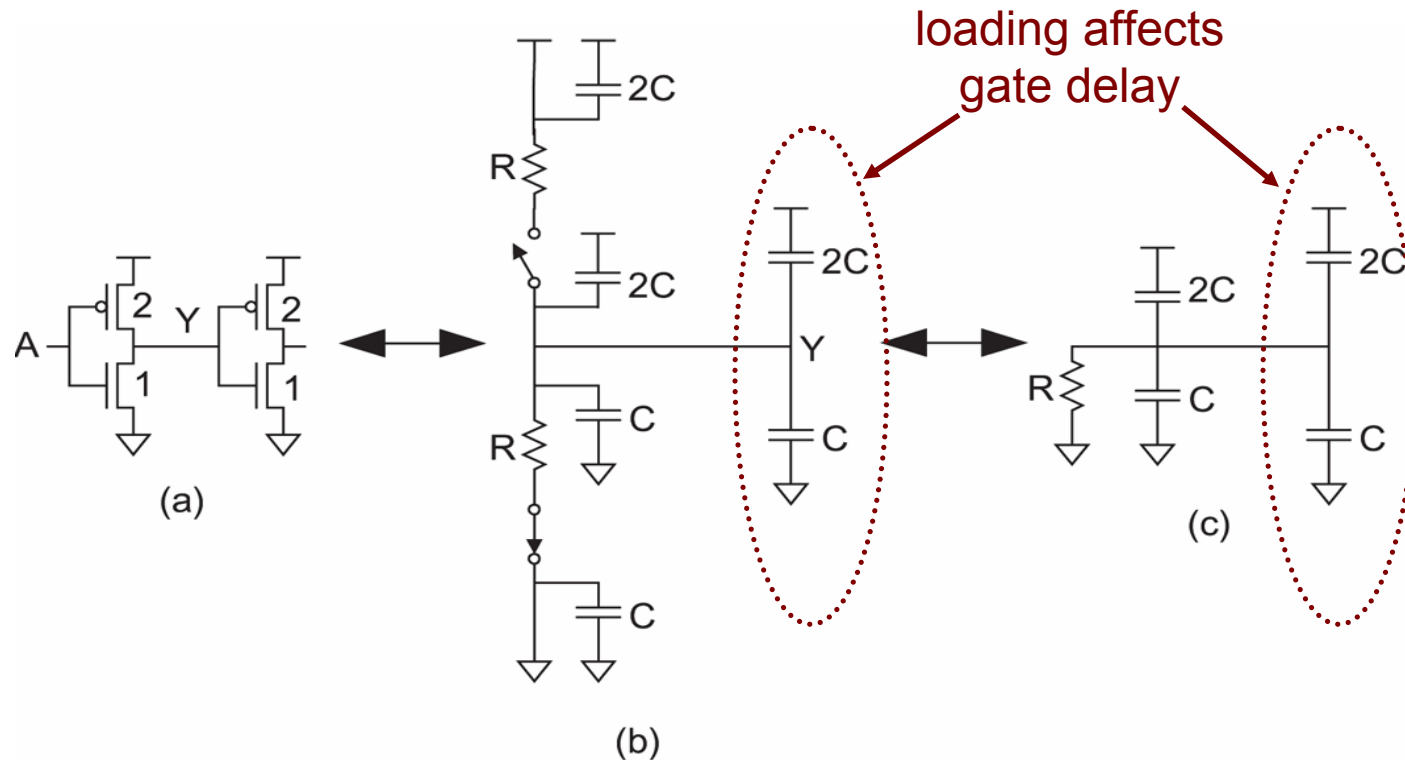
[see Gupta/Pileggi'97 for more info]

# Switch-level device RC delay models



[source: Weste/Harris]

# Modeling the delay of an inverter

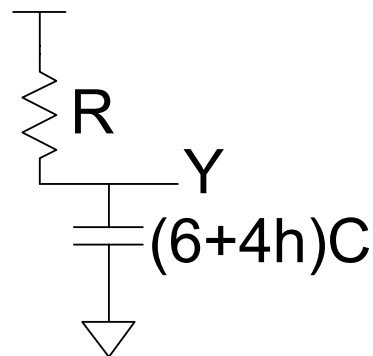
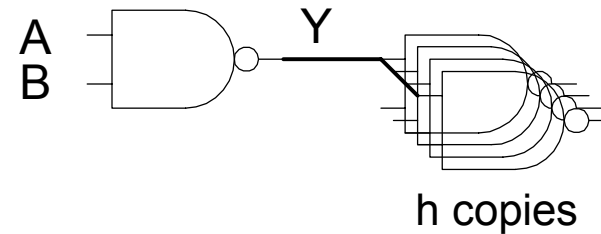
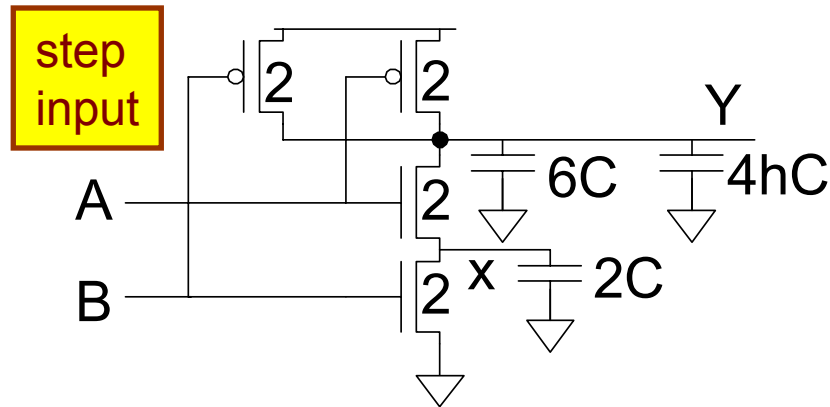


Holes have **half** the mobility of electrons

→ PMOS width =  $2\times$  of the NMOS device to get the same current (or resistance) during output rise

→ equal rise and fall delays for CMOS inverter

# Gate delay: rise delay



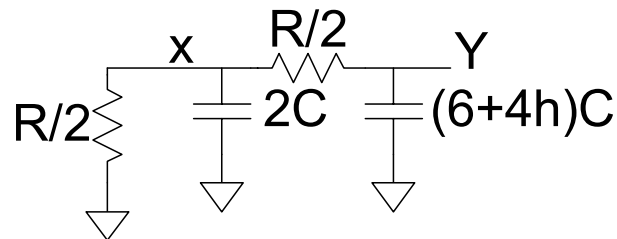
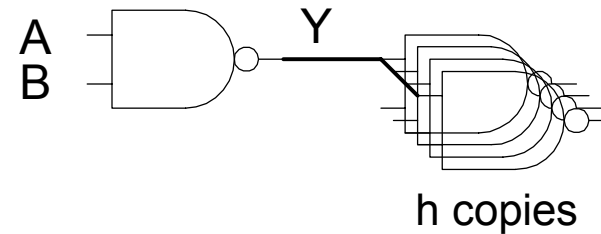
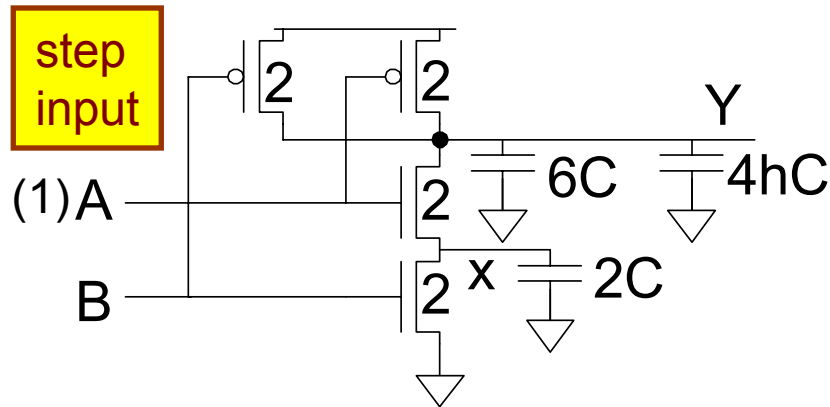
rise propagation delay

$$t_{pdr} = (6 + 4h)RC$$

Assumption: interconnect delay is ignored (for the moment)



# Gate delay: fall delay



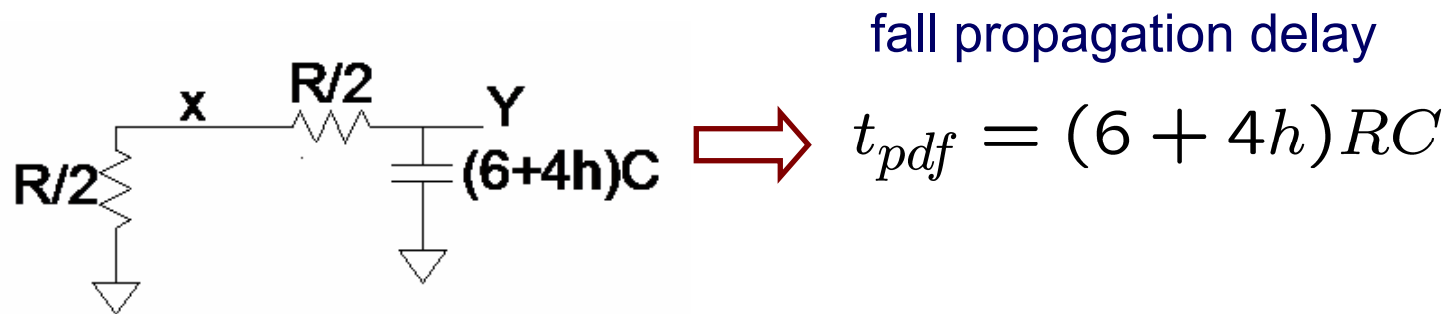
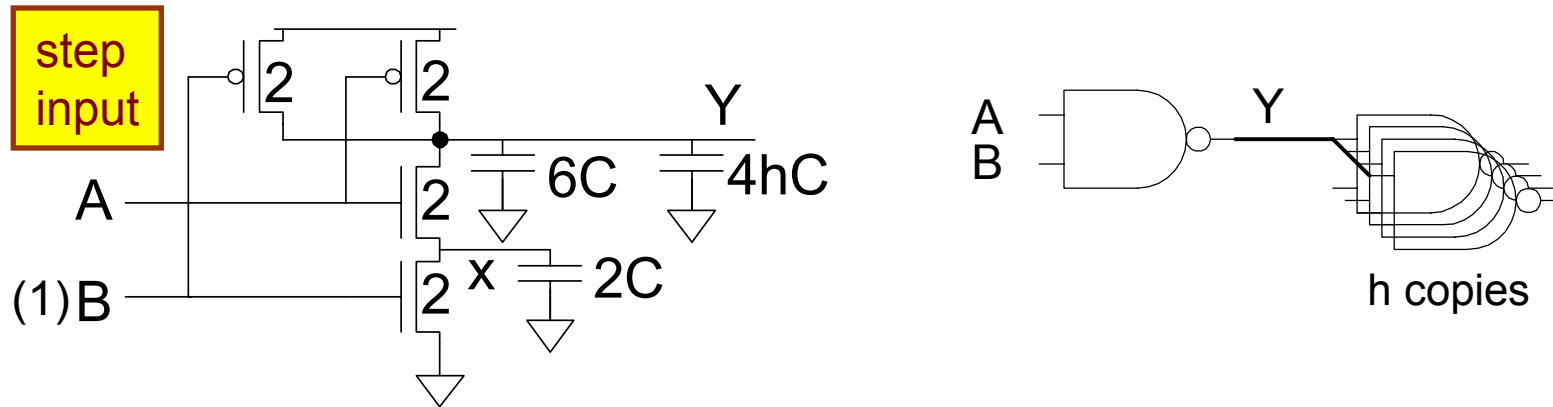
fall propagation delay

$$t_{pdf} = (2C)\left(\frac{R}{2}\right) + [(6 + 4h)C]\left(\frac{R}{2} + \frac{R}{2}\right)$$

$$= (7 + 4h)RC$$

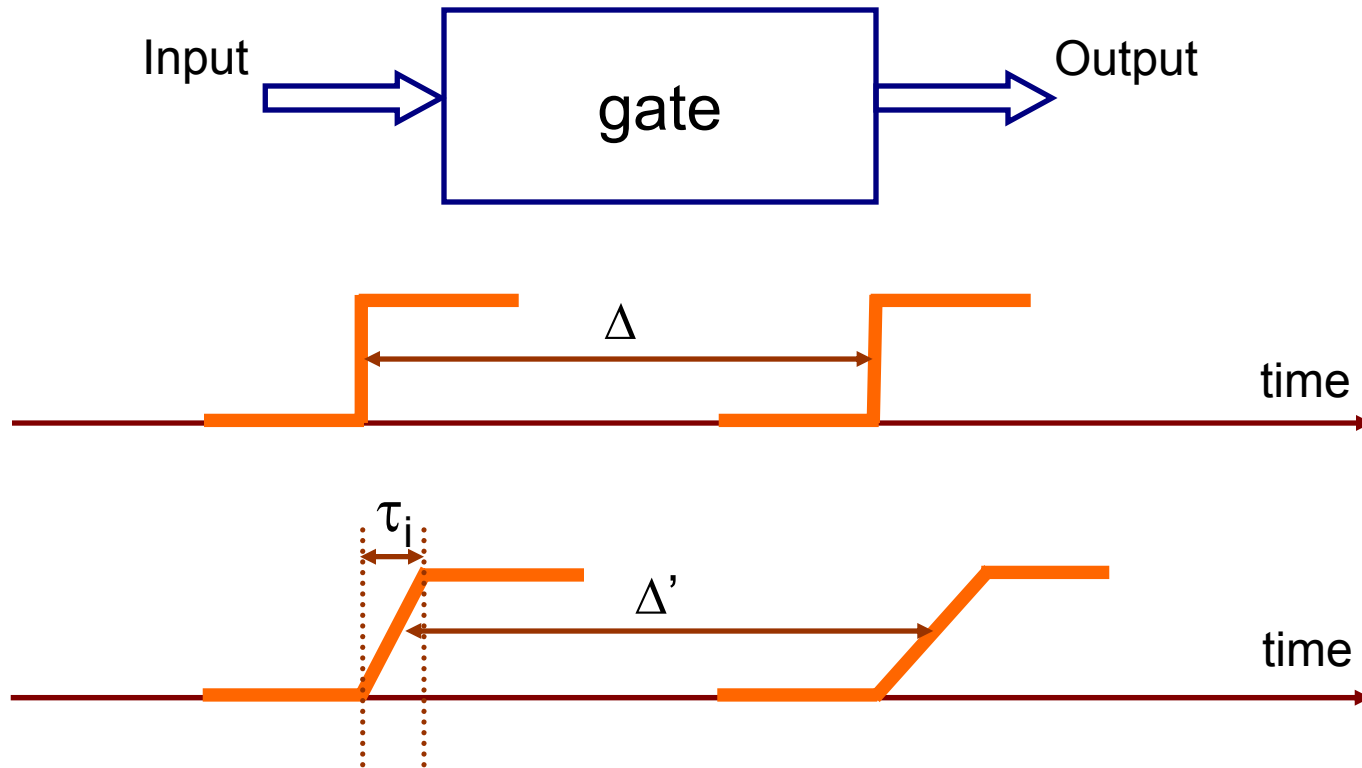
fall delay is worse than rise delay in this case

# Gate delay is input pattern dependant



⇒ Connect the latest arriving signal closest to the output node whenever feasible

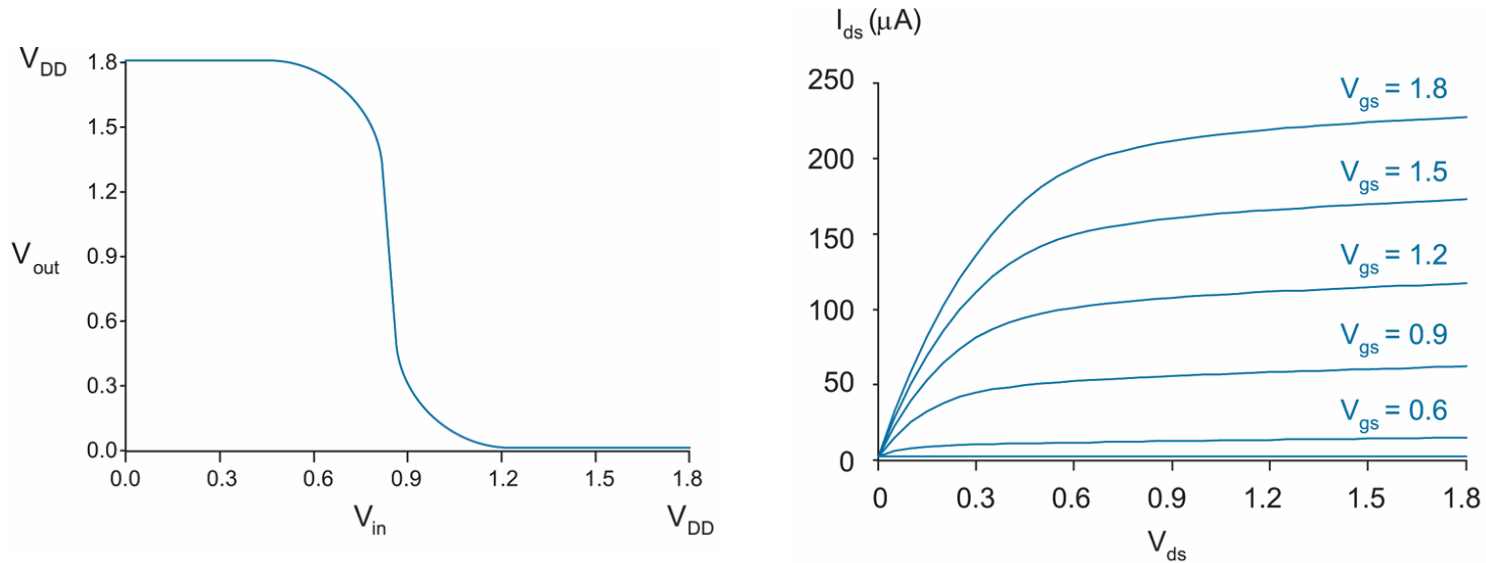
# Impact of transition time on gate delay



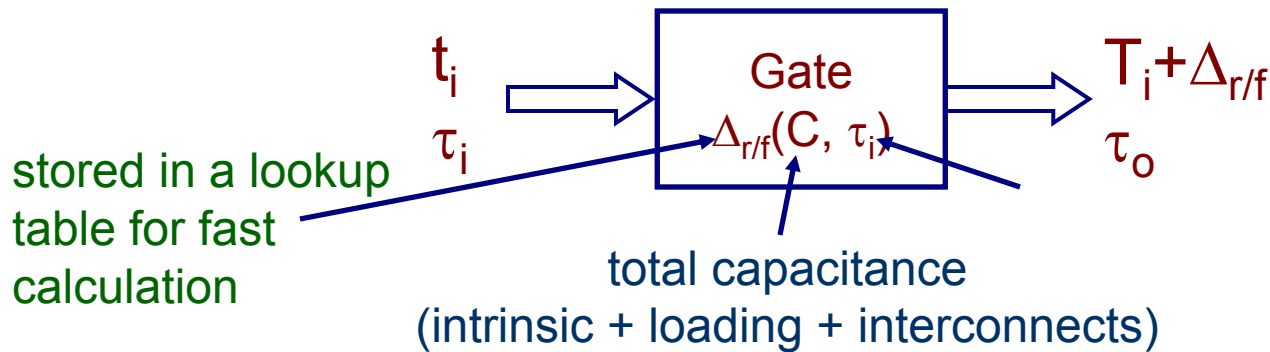
In addition to capacitive load, input transition time affects

- delay:  $\tau_i > 0 \rightarrow \Delta' > \Delta$
- output transition time:

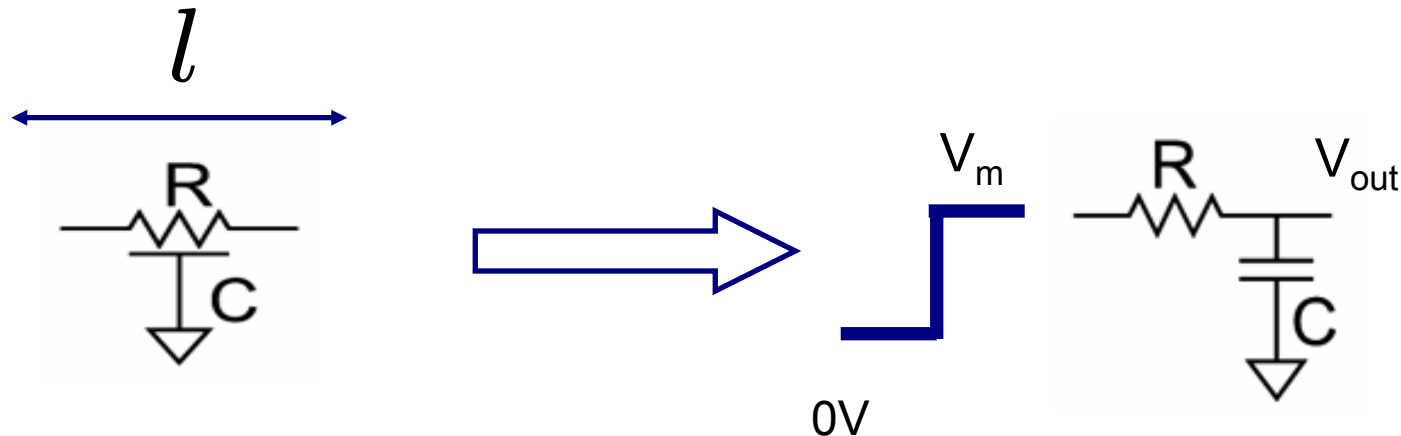
# Why does transition time affect delay?



During transition, gate current < saturation current  
 → higher effective output resistance → larger delay  
 ∴ Input transition time affects gate delay (and output transition time too!)



# Interconnect delay: the lumped case



$$V_{out} = V_m(1 - e^{-\frac{t}{RC}})$$

$$\frac{V_m}{2} = V_m(1 - e^{-\frac{t_{pd}}{RC}})$$

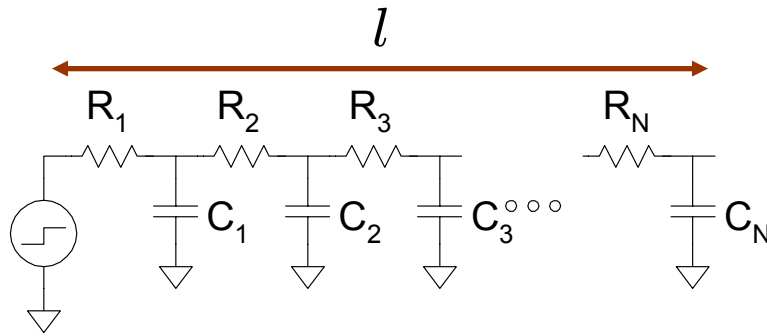
$$e^{-\frac{t_{pd}}{RC}} = \frac{1}{2}$$

$$t_{pd} = 0.69RC$$

$$\text{Elmore delay} = RC$$

Upper bound on  
delays in RC  
trees [Pileggi'97]

# Interconnect delay: lumped vs. distributed



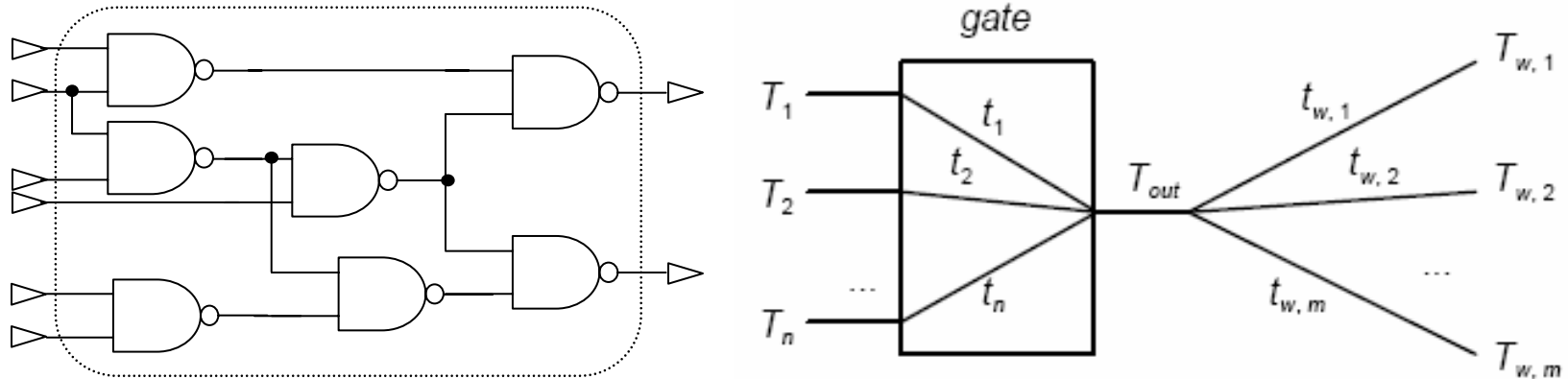
$$R_i = \frac{rl}{N} \quad r = \text{resistance per unit length}$$

$$C_i = \frac{cl}{N} \quad c = \text{capacitance per unit length}$$

- $t_{pd} \sim R_1(C_1 + \dots + C_N) + \dots + R_N C_N$
- $t_{pd} \sim \frac{rl}{N} \left( \frac{cl}{N} \times N \right) + \frac{rl}{N} \left( \frac{cl}{N} \times (N-1) \right) + \dots + \frac{rl}{N} \frac{cl}{N}$
- $t_{pd} \sim rc \left( \frac{l}{N} \right)^2 (N + N - 1 + \dots + 1)$
- $t_{pd} \sim rc \left( \frac{l}{N} \right)^2 \frac{N(N+1)}{2} \sim rcl^2 \frac{N+1}{2N} \sim \frac{rcl^2}{2}$



# Carryout STA after annotating your circuit with gate/interconnect delays



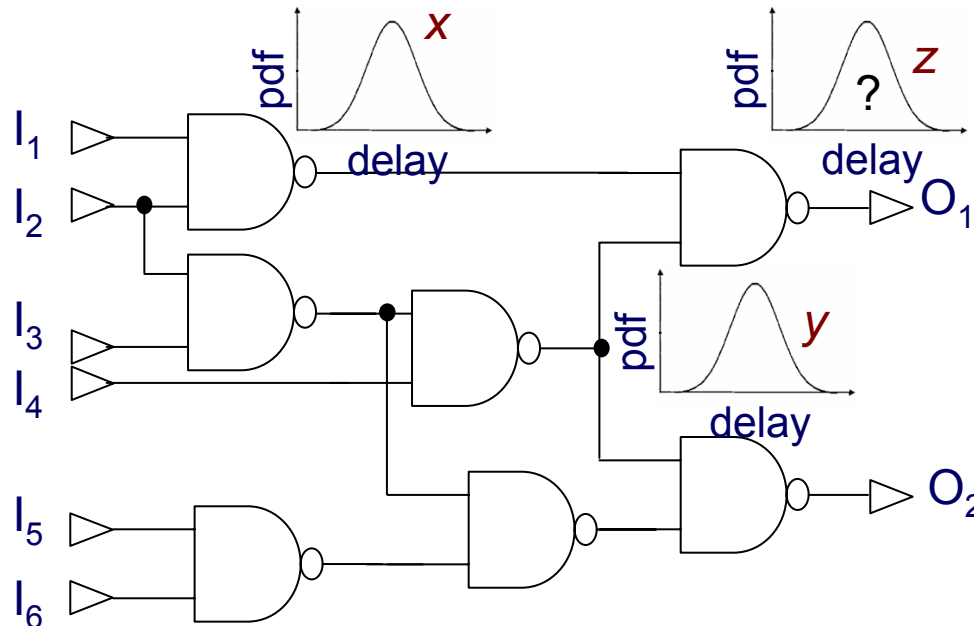
- Annotate your circuit with gate/interconnect delay, and carry out STA
- Don't ignore interconnect delay because it is currently responsible for ~80% of total path delays!

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# In Statistical STA (SSTA), delay is no longer deterministic

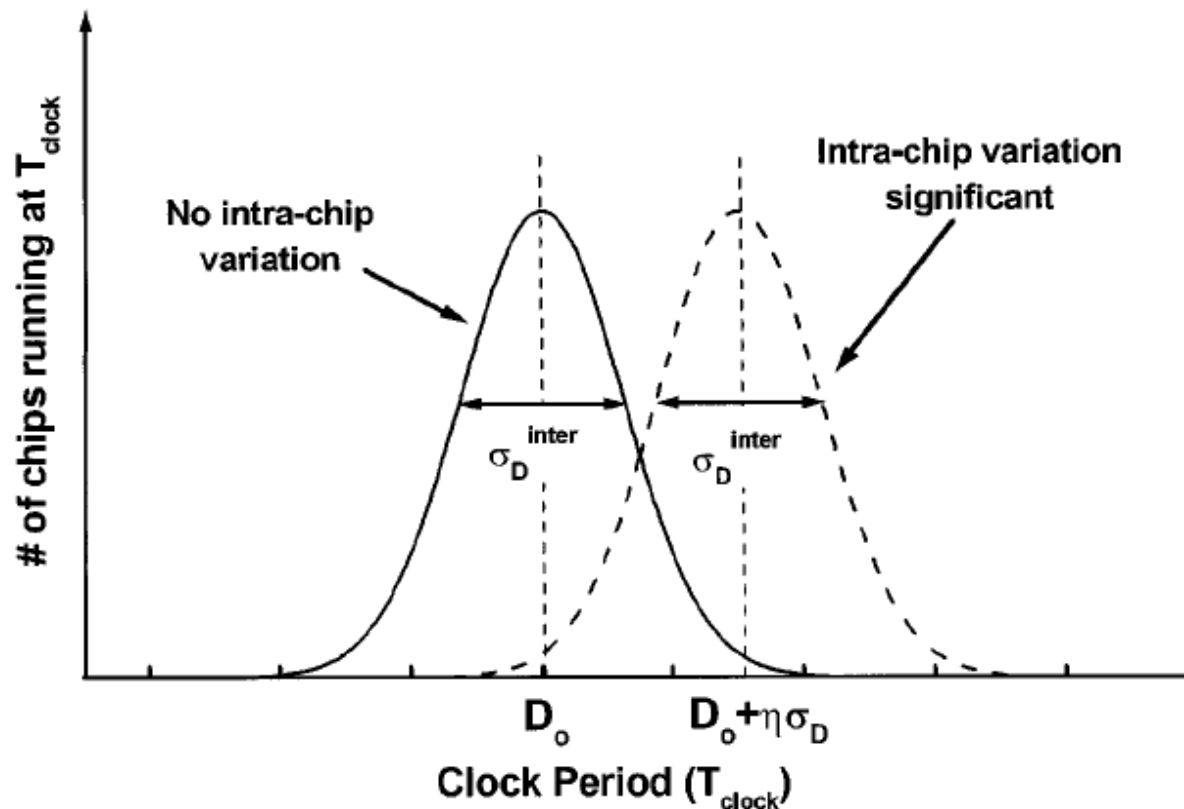


- Replace deterministic gate delay by a random delay variable that has a normal pdf
- What is the pdf of  $z = \max(x, y)$ , where  $x$  and  $y$  are two random normal variables?
  - $z$  is not normal, but can be approximated reasonable using random variables [Jacobs/Berkelaar'00]



# Gate variations impact critical path(s) delay leading to an increase in the *average* delay

- Intra-chip (within-die) variations: arises within devices in the same die
- Inter-chip (die-to-die) variations: arises between different chips



# Assignments for next lecture

## Reading assignments:

- [Statistical Timing Analysis for Intra-Die Process Variations with Spatial Correlations](#), ICCAD'03 (Kundan + (Yiwen) (judge))
- Incremental timing analysis, US Patent 5508937 (Cesare)
- Industrial products:
  - Cadence SignalStorm (Elif)
  - Synopsys PrimeTime (Brendan)

## Projects overview:

- 10-15 mins presentation on previous work + proposal
- 1½ → 2 page report